CNTFET-Based Design of Ternary Logic Gates and Arithmetic Circuits

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***Abstract*—This paper presents a novel design of ternary logic gates using carbon nanotube (CNT) FETs (CNTFETs). Ternary logic is a promising alternative to the conventional binary logic design technique, since it is possible to accomplish simplicity and energy efficiency in modern digital design due to the reduced circuit overhead such as interconnects and chip area. A resistive-load CNTFET-based ternary logic design has been proposed to implement ternary logic based on CNTFET. In this paper, a novel design technique for ternary logic gates based on CNTFETs is proposed and compared with the existing resistive-load CNTFET logic gate designs. Especially, the proposed ternary logic gate design technique combined with the conventional binary logic gate design technique provides an excellent speed and power consumption characteristics in datapath circuit such as full adder and multiplier. Extensive simulation results using SPICE are reported to show that the proposed ternary logic gates consume significantly lower power and delay than the previous resistive-load CNTFET gates implementations. In realistic circuit application, the utilization of the proposed ternary gates combined with binary gates results in over 90% reductions in terms of the power delay product.**

***Index Terms*—Carbon nanotube (CNT) FET (CNTFET), multiple-valued logic (MVL) design.**

I. Introduction

TRADITIONALLY, digital computation is performed on two-valued logic, i.e., there are only two possible values (0 or 1, true or false) in the Boolean space. Multiple-valued logic (MVL) replaces the classical Boolean characterization of variables with either finitely or infinitely many values such as ternary logic [1] or fuzzy logic [2]. Ternary logic (or three-valued logic) has attracted considerable interest due to its potential advantages over binary logic for designing digital systems. For example, it is possible for ternary logic to achieve simplicity and energy efficiency in digital design since the logic reduces the complexity of interconnects and chip area [3]. Furthermore, serial and serial-parallel arithmetic operations can be carried out faster if the ternary logic is employed. Extensive research on the design and implementation of ternary logic using CMOS can be found in the technical literature [3], [4]. Chip area and power dissipation can be reduced by more than 50% using an efficient MVL implementation for a signed 32-bits multiplier compared to its fastest binary counterpart [5]. MVL modules have been inserted into binary logic ICs to enhance the performance of CMOS technologies [6].

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There are two kinds of MVL circuits based on MOS technology, namely the current-mode MVL circuits and the voltage-mode MVL circuits. Voltage-mode MVL circuits have been achieved in multithreshold CMOS design [7]. The carbon nanotube (CNT) FET (CNTFET) is a promising alternative to the bulk silicon transistor for low-power and high-performance design due to its ballistic transport and low OFF-current properties [8]–[12]. A multithreshold CMOS design relies on body effects using different bias voltages to the base or the bulk terminal of the transistors. In a CNTFET, the threshold voltage of the transistor is determined by the diameter of the CNT. Therefore, a multithreshold design can be accomplished by employing CNTs with different diameters (and, therefore, chirality) in the CNTFETs. A resistive-load CNTFET-based ternary logic design has been proposed in [5]. However, in this configuration, large OFF-chip resistors (of at least 100 MΩ values) are needed due to the current requirement of the CNTFETs. The design technique proposed in this paper relies on [21] and eliminates the large resistors by employing active load with p-type CNTFETs in the ternary logic gates. In this paper, the multivalued logic design based on multithreshold CNTFETs is assessed and compared with existing multivalued logic designs based on CNTFETs.

The designs of basic ternary gates/operators (inverters, NAND, and NOR) are described in detail, and ternary full adder, and multiplier designs and analysis are presented as examples of the application of these ternary gates design technique. For the arithmetic circuit design, a modified ternary logic circuit design technique is used to speed up and reduce power consumption of the circuits. The modified ternary logic design uses both ternary logic gates and binary logic gates based on the previous ternary logic design structures to take advantage of the two logic design styles' merits. The ternary logic gates are a good candidate for decoding block since it requires less number of gates while binary logic gates are a good candidate for fast computation. In this paper, the modified ternary logic design method is proposed along with extensive simulation data. SPICE simulation results show substantial advantages in terms of speed and power consumption when the new CNTFET-based gates are employed for arithmetic circuit design.

II. Review of Ternary Logic

Ternary logic functions are defined as those functions having significance if a third value is introduced to the binary logic. In this paper, 0, 1, and 2 denote the ternary values to represent false, undefined, and true, respectively. Any n variable $\{X_1, \ldots, X_n\}$ ternary function $f(X)$ is defined as a logic function mapping $\{0, 1, 2\}^n$ to {0, 1, 2}, where $X = \{X_1, \ldots, X_n\}$. The basic operations of ternary logic can be defined as follows, where

TABLE I
LOGIC SYMBOLS

Voltage Level	Logic Value
0	0
1/2 V_{dd}	1
V_{dd}	2

TABLE II
TRUTH TABLE OF STI, PTI, AND NTI

Input X	STI	PTI	NTI
0	2	2	2
1	1	2	0
2	0	0	0

$X_i, X_j = \{0, 1, 2\}$ [13]:

$$\begin{aligned} X_i + X_j &= \max\{X_i, X_j\} \\ X_i \bullet X_j &= \min\{X_i, X_j\} \\ \overline{X_i} &= 2 - X_i \end{aligned} \tag{1}$$

where $-$ denotes the arithmetic subtraction, the operations $+$, $\bullet$, and are referred to as the OR, AND, and NOT in ternary logic, respectively.

The fundamental gates in the design of digital systems are the inverter, the NOR gate, and the NAND gate. The assumed logic symbols are shown in Table I. The ternary gates are designed according to the convention defined by (1).

A. Ternary Inverter

A general ternary inverter is an operator (gate) with one input x, and three outputs (denoted by y_0, y_1, and y_2) such that

$$\begin{aligned} y_0 &= C_0(x) = \begin{cases} 2, & \text{if } x = 0 \\ 0, & \text{if } x \neq 0 \end{cases} \\ y_1 &= C_1(x) = \overline{x} = 2 - x \\ y_2 &= C_2(x) = \begin{cases} 2, & \text{if } x \neq 2 \\ 0, & \text{if } x = 2. \end{cases} \end{aligned} \tag{2}$$

Therefore, the implementation of ternary inverter requires three inverters, and they are a negative ternary inverter (NTI), a standard ternary inverter (STI), and a positive ternary inverter (PTI), if y_0, y_1, and y_2 in (2) are the outputs [3]. The truth table of the three ternary inverters is shown in Table II.

B. Ternary NOR and NAND Gates

The ternary NAND and NOR are two multiple entry operators used in ternary logic. The functions of the two-entry ternary NAND and NOR gates are defined by the following two equations, respectively [4]:

$$Y_{\mathrm{NAND}} = \overline{\min\{X_1, X_2\}} \tag{3}$$

$$Y_{\mathrm{NOR}} = \overline{\max\{X_1, X_2\}}. \tag{4}$$

TABLE III
TRUTH TABLE OF NAND AND NOR

Input X_1	Input X_2	Y_{NAND}	Y_{NOR}
0	0	2	2
1	0	2	1
2	0	2	0
0	1	2	1
1	1	1	1
2	1	1	0
0	2	2	0
1	2	1	0
2	2	0	0

The truth table for the ternary NAND and NOR gates is shown in Table III.

III. CARBON NANOTUBE FET

CNTFETs utilize semiconducting single-wall CNTs to assemble electronic devices [8]. A single-wall CNT (or SWCNT) consists of one cylinder only, and the simple manufacturing process of this device makes it very promising for alternative to today's MOSFET. An SWCNT can act as either a conductor or a semiconductor, depending on the angle of the atom arrangement along the tube. This is referred to as the chirality vector and is represented by the integer pair (n, m). A simple method to determine if a CNT is metallic or semiconducting is to consider its indexes (n, m): the nanotube is metallic if $n = m$ or $n - m = 3i$, where i is an integer. Otherwise, the tube is semiconducting. The diameter of the CNT can be calculated based on the following [14]–[16]:

$$D_{\mathrm{CNT}} = \frac{\sqrt{3}a_0}{\pi}\sqrt{n^2 + m^2 + nm} \tag{5}$$

where $a_0 = 0.142$ nm is the interatomic distance between each carbon atom and its neighbor. Fig. 1 shows the schematic diagram of CNTFET [14]–[16]. Similar to the traditional silicon device, the CNTFET also has four terminals. As shown in Fig. 1, undoped semiconducting nanotubes are placed under the gate as channel region, while heavily doped CNT segments are placed between the gate and the source/drain to allow for a low series resistance in the ON-state [8]. As the gate potential increases, the device is electrostatically turned on or off via the gate.

The I–V characteristics of the CNTFET are similar to MOSFET's. The threshold voltage is defined as the voltage required to turn ON transistor. The threshold voltage of the intrinsic CNT channel can be approximated to the first order as the half bandgap that is an inverse function of the diameter [14]–[16], i.e.

$$V_{\mathrm{th}} \approx \frac{Eg}{2e} = \frac{\sqrt{3}}{3}\frac{aV\pi}{eD_{\mathrm{CNT}}} \tag{6}$$

where $a = 2.49$ Å is the carbon to carbon atom distance, $V_\pi = 3.033$ eV is the carbon π–π bond energy in the tight

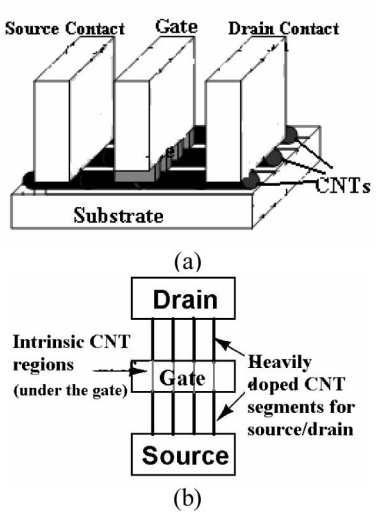

Fig. 1. Schematic diagram of a CNT transistor. (a) Cross sectional view. (b) Top view.

bonding model, e is the unit electron charge, and $D_{\rm CNT}$ is the CNT diameter. As $D_{\rm CNT}$ of a (19, 0) CNT is 1.487 nm, the threshold voltage of a CNTFET using (19, 0) CNTs as channels is 0.293 V from (6). Simulation results have confirmed the correctness of this threshold voltage. As the chirality vector changes, the threshold voltage of the CNTFET will also change. Assume that m in the chirality vector is always zero, then the ratio of the threshold voltages of two CNTFETs with different chirality vectors is given as:

$$\frac{V_{\rm th1}}{V_{\rm th2}} = \frac{D_{\rm CNT2}}{D_{\rm CNT1}} = \frac{n_2}{n_1}. \tag{7}$$

Equation (7) shows that the threshold voltage of a CNTFET is inversely proportional to the chirality vector of the CNT. For example, the threshold voltage of a CNTFET using (13, 0) CNTs is 0.428 V, compared to a (19, 0) CNTFET with a threshold voltage of 0.293 V. Using HSPICE simulation, the drain current of CNTFET with (19, 0) chirality at the threshold voltage calculated by (6) is found, and it is used as the reference transistor ON-current. The gate-to-source voltage that generates the same reference current is taken as the threshold voltage for the transistor that has different chirality. Fig. 2 shows the threshold voltage of both PCNTFET and NCNTFET obtained from (6), and HSPICE simulation for various chirality vectors (various n for $m = 0$). CNTFETs provide a unique opportunity to control threshold voltage by changing the chirality vector, or the diameter of the CNT [5]. Li *et al.* [17] and Ohno *et al.* [18] have reported advances on manufacturing processes for well-controlled CNTs. A synthesis process for fabricating SWCNTs with the desired (*n, m*) chirality structure has been proposed in [22]. Lin *et al.* [23] have demonstrated postprocessing techniques to adjust the threshold voltage of multiple-tube CNTFETs. In this paper, we use a multidiameter CNTFET-based design for ternary logic implementation.

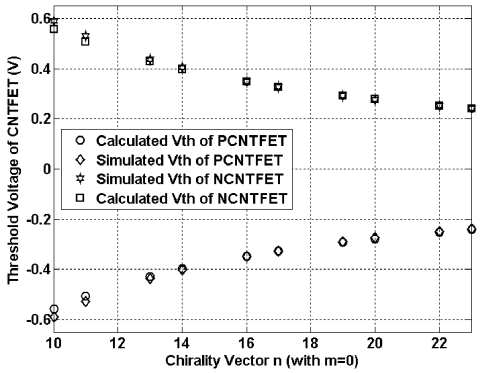

Fig. 2. Threshold voltage of CNTFETs versus n (for $m = 0$).

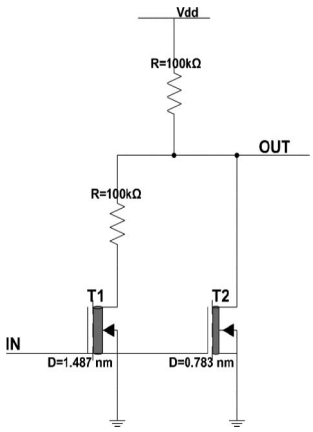

Fig. 3. Schematic diagram of CNTFET-based STI proposed in [5].

IV. CNTFET-Based Ternary Inverter Design

A. Existing Design

A CNTFET-based ternary logic design has been initially proposed in [5]. It employs dual-diameter CNTFETs and resistors. Fig. 3 shows the schematic diagram of the STI discussed previously in Section II. It consists of two CNTFETs with resistive pull-ups. In this paper, a power supply voltage of 0.9 V (as default value of the CNTFET model of [14]) is used. Therefore, logic 0 corresponds to a voltage value less than 0.3 V, logic 1 corresponds to a voltage value between 0.3 and 0.6 V, and logic 2 corresponds to a voltage value greater than 0.6 V. In Fig. 3, one of the transistors (T1) has a diameter $d_1 = 1.487$ nm, while the other transistor (T2) has a diameter $d_2 = 0.783$ nm. Therefore, the two transistors have threshold voltages of $V_{\rm th1} =$ 290 mV and $V_{\rm th2} = 550$ mV, respectively. When the input voltage is lower than 300 mV, both T1 and T2 are OFF, and the output voltage is 900 mV. As the input voltage increases beyond 300 mV, T1 is ON and T2 is still OFF, and the output voltage is held approximately at $V_{\rm dd}/2$ until the input voltage reaches $V_{\rm th2}$. Once the input voltage exceeds $V_{\rm th2}$, both T1 and T2 are ON and the output voltage is pulled down to nearly zero. By choosing CNTFETs with proper threshold voltages, a ternary logic inverter design is achieved. However, as shown in Fig. 3, two large resistors (usually 100 MΩ or greater) are required to

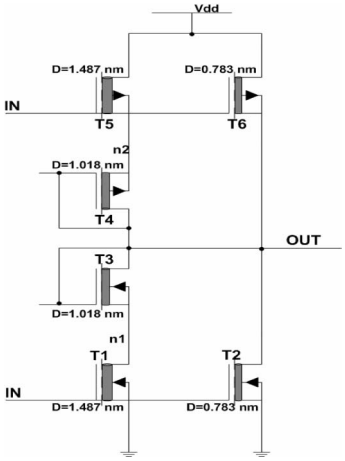

Fig. 4. Proposed CNTFET-based STI design.

implement the design of [5], but their values are too large to be integrated into CNTFET technology.

B. Proposed CNTFET-Based Design

One of the most widely used logic design style is static complementary CMOS; the main advantages of the complementary design are robustness, good performance, and low power consumption with small static power dissipation. A complementary CNTFET network can also be used for ternary logic design to achieve good performance, low power consumption, and to avoid the use of large resistors and reduce area overhead. Fig. 4 shows the proposed CNTFET-based STI design; the STI in Fig. 4 consists of six CNTFETs. The chiralities of the CNTs used in T1, T2, and T3 are (19, 0), (10, 0), and (13, 0), respectively. From (5), the diameters of T1, T2, and T3 are 1.487, 0.783, and 1.018 nm, respectively. Therefore, the threshold voltages of T1, T2, and T3 are 0.289, 0.559, and 0.428 V, respectively from (6). The threshold voltages of T5, T6, and T4 are -0.289, -0.559, and -0.428 V, respectively. When the input voltage changes from low to high at the power supply voltage of 0.9 V, initially, the input voltage is lower than 300 mV. This makes both T5 and T6 turn ON, both T1 and T2 turn OFF, and the output voltage 0.9 V, i.e. logic 2. As the input voltage increases beyond 300 mV, T6 is OFF and T5 is still ON. Meanwhile, T1 is ON and T2 is OFF. The diode connected CNTFETs T4 and T3 produce a voltage drop of 0.45 V from node n2 to the output, and from the output to n1 due to the threshold voltages of T4 and T3. Therefore, the output voltage becomes 0.45 V, i.e., half of the power supply voltage. As shown in Table I, half $V_{\rm dd}$ represents logic 1. Once the input voltage exceeds 0.6 V, both T5 and T6 are OFF, and T2 is ON to pull the output voltage down to zero. The input voltage transition from high to low transition is similar to the low to high transition.

Simulation on these STIs has been performed by HSPICE using the CNTFET model of [14]. This HSPICE model of the CNTFET is described in more detail in [15] and [16]. The voltage transfer characteristics (VTCs) of the STI in Figs. 3 and 4 are shown in Fig. 5(a) and (b), respectively. Compared with the STI design in Fig. 3, the proposed STI design provides a larger

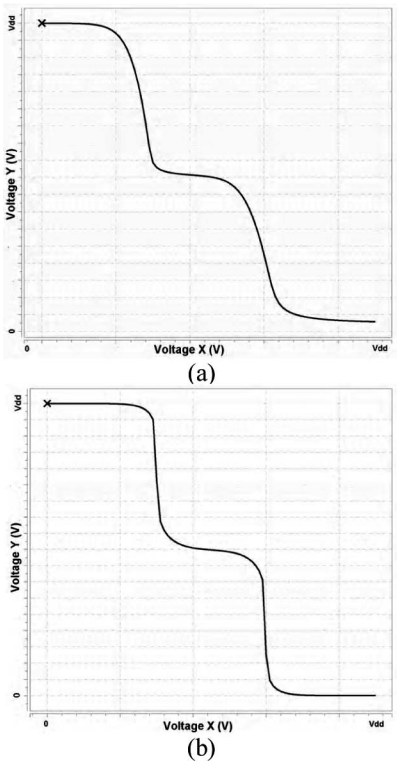

Fig. 5. VTC of STI. (a) STI in Fig. 3. (b) STI in Fig. 4.

noise margin, which is a positive feature for low-power supply circuits. Furthermore, the proposed STI achieves a rail-to-rail output swing in contrast to the STI design shown in Fig. 3. HSPICE simulation has been performed to investigate the performance of the CNTFET-based STI. As a very important metric for digital circuits, the power delay product (PDP) is used for the CNTFET-based STI. The PDP is the product of the average power consumption and the average delay. In the HSPICE simulation, two STIs are cascaded as a ternary buffer. The average power consumption is the average power consumed by the two STIs, while the average delay is the average of the sum of four terms, i.e., the delay from 0 to 1, the delay from 1 to 2, the delay from 2 to 1, and the delay from 1 to 0. HSPICE simulation shows that the PDP of the proposed CNTFET-based STI is 6.08e $-$ 17 J, and the PDP of the STI in [5] is 2.07e $-$ 16 J. The proposed CNTFET-based STI achieves more than 300% performance improvement over [5] in terms of PDP.

V. Ternary Gate Design

As mentioned in the Section II, there are three inverters in the general ternary inverter system, which are NTI, STI, and PTI [3]. Fig. 4 shows the proposed STI design. The NTI and PTI designs are shown in Fig. 6, where Fig. 6(a) shows the CNTFET-based NTI schematic diagram. The threshold voltage of T1 is 0.289 V, while the threshold voltage of T2 is -0.557 V. When the input voltage is below 0.3 V (i.e., logic 0), the output voltage is 0.9 V. As soon as the input voltage exceeds 0.3 V, T1 is ON and T2 is OFF, and the output voltage will be zero. For the CNTFET-based

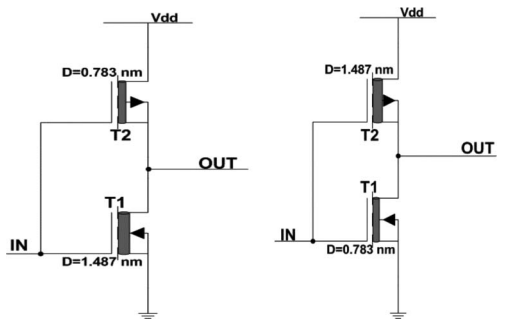

Fig. 6. Schematic diagram of (a) NTI and (b) PTI.

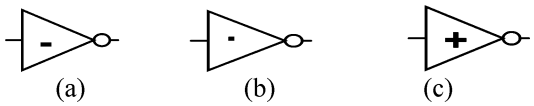

Fig. 7. Symbols of (a) NTI, (b) STI, and (c) PTI.

PTI shown in Fig. 6(b), the threshold voltage of T1 is 0.557 V and the threshold voltage of T2 is -0.289 V. Therefore, only when the input voltage is higher than 0.6 V, the output voltage is zero. The outputs of NTI and PTI correspond to y_0 and y_2, as given previously in (2). Fig. 7 shows the symbols of NTI, STI, and PTI.

The logic expressions of the ternary NAND and NOR gates are given in (3) and (4). The circuits and symbols for the two-input ternary NAND and ternary NOR are shown in Fig. 8(a) and (b), respectively. Each of these two gates consists of ten CNTFETs, with three different chiralities. They are essentially the same as their binary CMOS counterparts, except for the transistors of different threshold voltages. In these two gates, similar to the STI circuit of Fig. 4, the transistors with diameters of 1.487, 0.783, and 1.018 nm have threshold voltages of 0.289, 0.559, and 0.428 V, respectively, as established using (6). HSPICE simulation has confirmed the correctness of these designs with Tables II and III.

VI. Basic Ternary Arithmetic Circuits

The ternary gates presented in the Section V can be used for designing ternary arithmetic circuits such as ternary adders and multipliers. As required for these circuits, a new design of the ternary decoder is presented in Fig. 9. The ternary decoder is a one-input, three-output combinational circuit and generates unary functions for an input x. The response of the ternary decoder to the input x is given by

$$X_k = \begin{cases} 2, & \text{if } x = k \\ 0, & \text{if } x \neq k \end{cases} \tag{8}$$

where k can take logic values of 0, 1, or 2. The decoder consists of a PTI gate, two NTI gates, and a NOR gate, as shown in Fig. 9.

One of the main advantages of ternary logic is that it reduces the number of required computation steps. Since each signal can have three distinct values, the number of digits required in a ternary family is $\log_3 2$ times less than required in binary

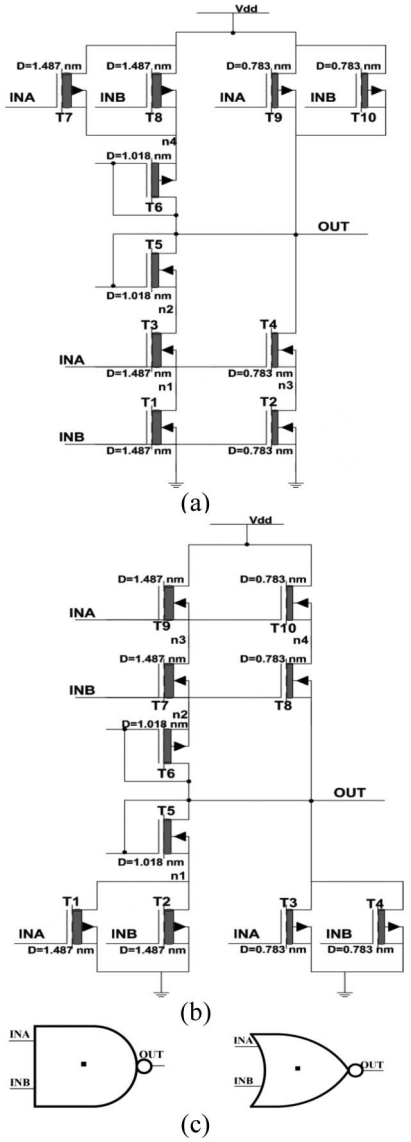

Fig. 8. Proposed CNTFET-based NAND and NOR gates. (a) Schematic diagram of two-input NAND. (b) Schematic diagram of two-input NOR. (c) Symbols of NAND and NOR.

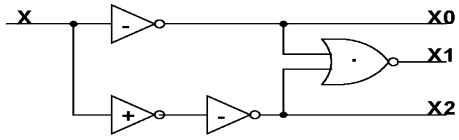

Fig. 9. Schematic diagram of ternary decoder.

logic. Therefore, if we consider an N-bit binary adder, then the corresponding ternary adder has $\lceil \log_3 2N \rceil$ digits, where $\lceil x \rceil$represents the integer nearest to x and greater than x (i.e., the ceiling function).

A ternary half adder (HA) is then designed to verify the correctness of the proposed CNTFET-based design. The truth table of the ternary adder is given in Table IV. The Karnaugh map of the HA is given in Table V. The output equations for the

TABLE IV
KARNAUGH MAP OF HA

Sum

A/B	0	1	2
0		1	2
1	1	2	
2	2		1

Carry

A/B	0	1	2
0			
1			1
2		1	1

TABLE V
TRUTH TABLE OF HA

A	B	Sum	Carry
0	0	0	0
0	1	1	0
0	2	2	0
1	1	2	0
1	2	0	1
2	2	1	1

HA can be derived from the Karnaugh map of Table V as

$$\text{Sum} = A_2B_0 + A_1B_1 + A_0B_2 + 1 \bullet (A_1B_0 + A_0B_1 + A_2B_2) \tag{9}$$

$$\text{Carry} = 1 \bullet (A_2B_1 + A_2B_2 + A_1B_2) \tag{10}$$

where A_k and B_k denote the output of the inputs A and B from the decoder shown in Fig. 9. The schematic diagram of the HA proposed in [20] is shown in Fig. 10. Two decoders generate the unary output signals for inputs A and B, while the logic gates (such as ANDs and ORs) compute the functions given by (9) and (10). The so-called T buffer of Fig. 10 represents a level shifter and its logic function is given by

$$\text{Out} = \begin{cases} 1, & \text{if in} = 1, 2 \\ 0, & \text{if in} = 0 \end{cases} \tag{11}$$

where in is the input of the T gate and Out is the output of the T gate. The transient response of the ternary HA design based on CNTFETs is shown in Fig. 12. Simulation results are consistent with the truth table given in Table IV.

As shown in Fig. 10, the design of [20] uses only ternary gates for the ternary HA. However, if the ternary and binary logic gates are used to take advantage of their respective merits, performance could be significantly improved because ternary logic (requiring a smaller number of transistors) is a good candidate for logic circuits such as a decoder, while binary logic is a good candidate for fast computing modules. The output of the decoder has only two logic values, i.e., 2 and 0, corresponding to logic 1 and 0 in binary logic. Therefore, binary gates can be

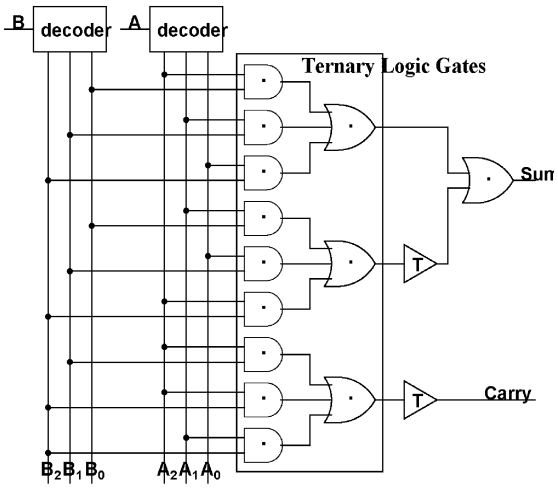

Fig. 10. Schematic diagram of ternary HA [20].

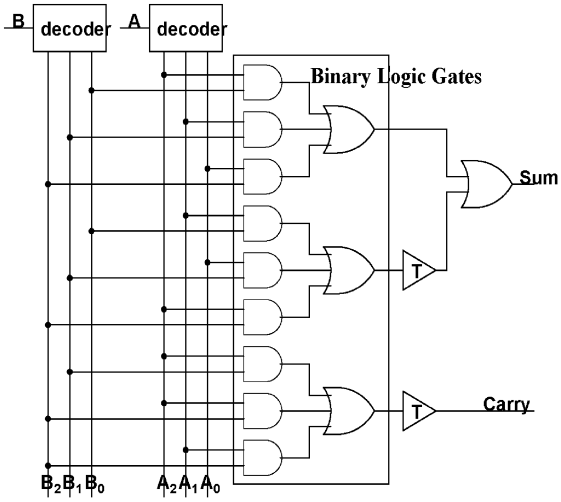

Fig. 11. Schematic diagram of proposed ternary HA.

used in a ternary circuit for accomplishing a faster operation. A modified ternary HA architecture is proposed in this paper, and is shown in Fig. 11. Simulation has been performed on the ternary HA circuit of Fig. 10, the ternary HA of Fig. 11, and the ternary HA using ternary gate family with resistors (proposed in [5]) at a 0.9-V power supply and room temperature. As marked in Fig. 12, the transition delays of t1, t2, t3, and t4 have been measured. For example, t1 is the delay from the rising edge "$0- > 1$" of input B to the rising edge "$0- > 1$" of the output Sum. The simulation results are shown in Fig. 13 to show the comparison among the three different adder implementations. Simulation on all implementations has been performed by HSPICE using the CNTFET model of [14]. Using binary gates, the proposed ternary HA is faster than the ternary adder of [20] and also faster than the ternary HA with pull-up resistors of [5]. The average power consumption of the ternary HAs has also been measured. The product of the average power consumption and the average transition delay of t1, t2, t3, and t4 yield the PDP of the ternary HAs. The PDPs of the three ternary HAs are given in Table VII for comparisons. The scheme utilizing the proposed

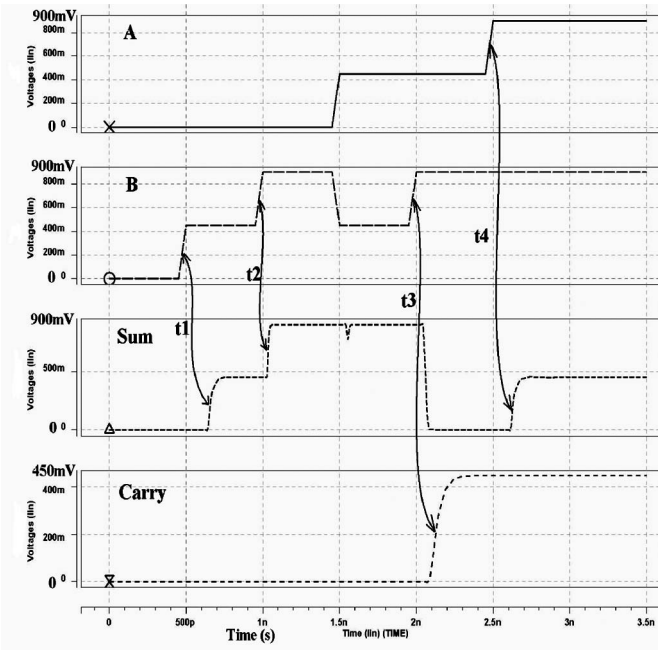

Fig. 12. Transient response of the ternary HA.

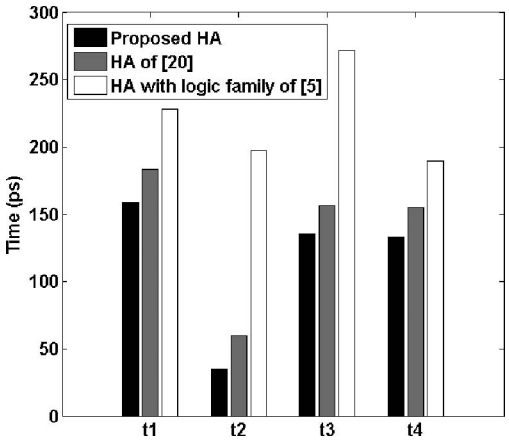

Fig. 13. Transient delay of CNTFET-based ternary HAs.

ternary logic achieves significant savings in PDP compared with the ternary logic family with resistors proposed in [5]. By replacing ternary gates with binary gates in the internal logic, the proposed design also achieves power and delay savings due to the reduced number of transistors in the binary gates. Note that by replacing the external resistors with transistors, a significant saving in area is also achieved. Therefore, the proposed ternary design is a fast and low-power solution to digital computation compared with the existing conventional ternary logic families, as well as the binary implementation (already proved in [5]).

A ternary multiplier has also been designed to evaluate the proposed logic family. The truth table of 1-bit multiplier is given in Table VI. The output equations of the 1-bit multiplier can be derived from the truth table as

$$\text{Product} = A_2B_1 + A_1B_2 + 1 \bullet (A_1B_1 + A_2B_2) \quad (12)$$

$$\text{Carry} = 1 \bullet (A_2 + B_2) \quad (13)$$

TABLE VI
TRUTH TABLE OF 1-BIT MULTIPLICATION

A	B	Product	Carry
0	0	0	0
0	1	0	0
0	2	0	0
1	1	1	0
1	2	2	0
2	2	1	1

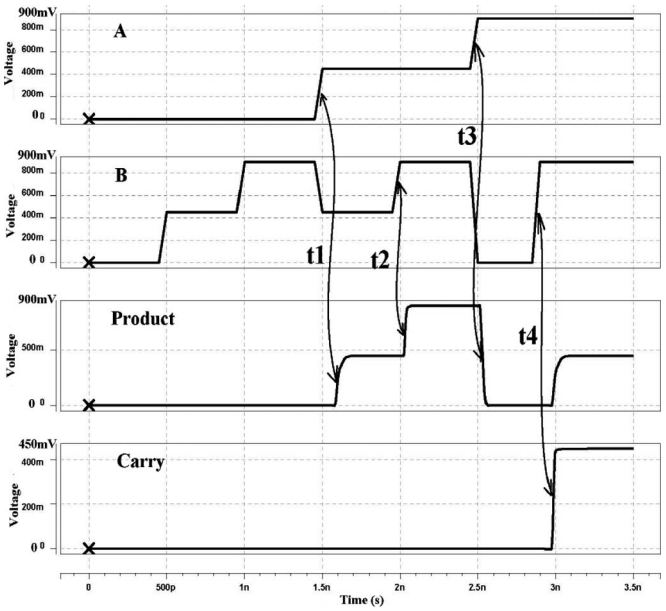

Fig. 14. Transient response of the ternary 1-bit multiplier.

where A_k and B_k denote the outputs of the inputs A and B from the decoder shown in Fig. 9. A 1-bit multiplier is built based on (12) and (13). Similar to the ternary adder design, binary logic gates can be used in the ternary design for higher speed. Simulation has also been performed on the multiplier of [20], the modified ternary multiplier with binary logic gates, and the ternary multiplier using a ternary logic family with resistors proposed in [5] at a 0.9-V power supply and room temperature. The transient responses of the 1-bit multiplier are shown in Fig. 14, and simulation results are also consistent with the truth table shown in Table VI. As marked in Fig. 14, the transition delays of t1, t2, t3, and t4 are measured. The simulation results for the transient delay are shown in Fig. 15. The average power consumption and average transition delay (over t1, t2, t3, and t4) are multiplied to find the PDP of the ternary multipliers. The PDPs of the three ternary multipliers are given in Table VII. The simulation results confirm that the proposed ternary logic design is a fast and low-power solution to digital computation compared with existing ternary logic families for arithmetic circuits.

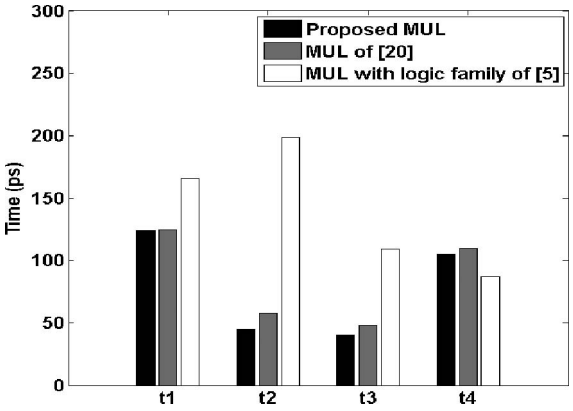

Fig. 15. Transient delay of CNTFET-based ternary multipliers.

TABLE VII
PDP OF ARITHMETIC CIRCUITS

Arithmetic circuit	Proposed circuit (J)	Circuit of [20] (J)	Circuit of [5] (J)
Half Adder	0.411e-15	0.543e-15	6.17e-15
Multiplier	0.248e-15	0.261e-15	2.62e-15

VII. CONCLUSION

This paper has presented the design of the new a ternary logic family based on CNTFETs. As the threshold voltage of the CNTFET is function of the geometry of the CNTFET (i.e., the chirality), a novel multidiameter (multithreshold voltage) CNTFET-based ternary design has been pursued in this paper. A complete set of ternary gates has been implemented using multidiameter CNTFETs. A few ternary arithmetic circuits such as the HA and multiplier have been also designed to show the effectiveness of the proposed ternary family for circuit design. Compared with previous CNTFET-based designs, the proposed ternary gates achieve high performance, low power, and small area due to the removal of resistors and the utilization of binary gates in the design of arithmetic circuits. All simulations have been performed in HSPICE using the CNTFET model provided by [14]. Simulation results have confirmed the power and delay improvements is possible by the proposed ternary logic family at both gate and circuit levels. The presented results show that the design approach using the ternary logic gate combined with binary gates is a viable solution for low-power and high-performance very large-scale integrated (VLSI) design with CNTFETs in nanoscale era.

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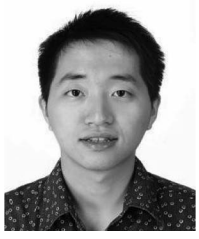

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