Design of a CNTFET-Based SRAM Cell by Dual-Chirality Selection

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***Abstract*—This paper proposes a new design of a highly stable and low-power static RAM (SRAM) cell using carbon nanotube FETs (CNTFETs) that utilizes different threshold voltages for best performance. In a CNT, the threshold voltage can be adjusted by controlling the chirality vector (i.e., the diameter). In the proposed six-transistor SRAM cell design, while all CNTFETs of the same type have the same chirality, n-type and p-type transistors have different chiralities, i.e., a dual-diameter design of SRAM cell. As figures of merit, stability, power dissipation, and write time are considered when selecting the chirality for the best overall performance. A new metric, denoted as "SPR," is proposed to capture these figures of merit. This metric shows that a CNTFET-based SRAM cell provides an "SPR" that is four times higher than for its CMOS counterpart that has the same configuration, thus attaining superior performance. Finally, the sensitivity of the CNTFET SRAM design to process variations is assessed and compared with its CMOS design counterpart. Extensive simulations have been performed to investigate the distribution of the power and delay of the CNTFET-based SRAM cell due to variations in the diameter, supply voltage, and temperature of the CNTFETs. The CNTFET-based SRAM cell demonstrates that it tolerates the process, power supply voltage, and temperature variations significantly better than its CMOS counterpart.**

***Index Terms*—Carbon nanotube FET (CNTFET), high performance, process variations, static RAM (SRAM) design, threshold voltage.**

I. Introduction

At nano-feature sizes, scaling has resulted in increased short-channel effects, reduced gate control, exponentially rising leakage currents, severe process variations, and high power density. As today's very large scale integration (VLSI) systems mostly rely on silicon MOS technology, the Industry Technology Roadmap (ITR) has predicted that in the nano regimes, the expected high density will encounter substantial difficulties in terms of physical phenomena and technology limitations, possibly preventing the continued improvements in figures of merit, such as low power and high performance. Nanoscaled alternatives to bulk silicon transistors are therefore being pursued. Ultrathin body devices such as FinFETs have received an increasing attention in recent years [1]. Furthermore, new materials and devices have been investigated to replace silicon in nanoscaled transistors from the year 2015 and beyond (as per ITR prediction). Carbon nanotube FETs (CNTFETs), for example, are promising due to their unique 1-D band structure that suppresses backscattering and makes near-ballistic operation a realistic possibility [2]–[5].

Design of fast and power-efficient memory structures continues to be of the highest priority, and ballistic transport operation and low OFF current make the CNTFET a suitable device for high performance and increased integration density of SRAM design. Moreover, the MOSFET-like model of the CNTFET is likely to be scaled down to 10 nm channel length, thus providing a substantial performance and power improvement compared to the MOSFET model (with minimum channel length of 32 nm [6]). Therefore, an SRAM design implemented using CNTFETs requires a significantly smaller area than its CMOS counterpart. A resistive-load CNTFET-based SRAM cell has been proposed in [7]. However, large off-chip resistors (i.e., 100 MΩ) are needed in the configuration due to the current requirements of the CNTFETs. This resistive-load CNTFET-based SRAM cell design is modified with p-type transistors as active load to address this problem, as proposed in this paper.

The use of transistors with multiple threshold voltages (i.e., a so-called multithreshold design) is widely utilized in today's CMOS circuits to improve performance. The threshold voltage can be changed by applying different bias voltages to the bulk terminal of the CMOS transistors. The threshold voltage of CNTFET is determined by the CNT diameter. Therefore, CNTFETs with different threshold voltages can be accomplished by growing CNTs with different diameters (chiralities). In this paper, a CNTFET-based SRAM cell design with optimized threshold voltages is proposed, assessed, and compared to the CMOS implementation of the same cell. Different diameters (and therefore, chirality) are utilized for the two types of CNTFETs (i.e., n or p). The optimum chirality is selected to achieve the best-combined performance in terms of stability, power consumption, and write time of the CNT-based SRAM cell. The write operation of the SRAM cells is evaluated using the novel comprehensive metric denoted as "SPR." The analysis and simulation for systematic and random process variations are also performed to demonstrate that the CNTFET memory cell is less susceptible to random variations than its CMOS counterpart.

II. Carbon Nanotube FET

CNTFETs utilize semiconducting single-wall CNTs (SWCNTs) to assemble electronic devices; CNTFETs have been shown to have properties similar to MOSFETs. An SWCNT consists of only one cylinder, and the simple manufacturing process of this device makes it a very promising alternative to today's MOSFET. An SWCNT can act as either a conductor or a semiconductor, depending on the angle of the atom arrangement along the tube. This is referred to as the chirality vector and is

Manuscript received January 24, 2009; revised May 16, 2009. First published June 16, 2009; current version published January 8, 2010. The review of this paper was arranged by Associate Editor C. Zhou.

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Digital Object Identifier 10.1109/TNANO.2009.2025128

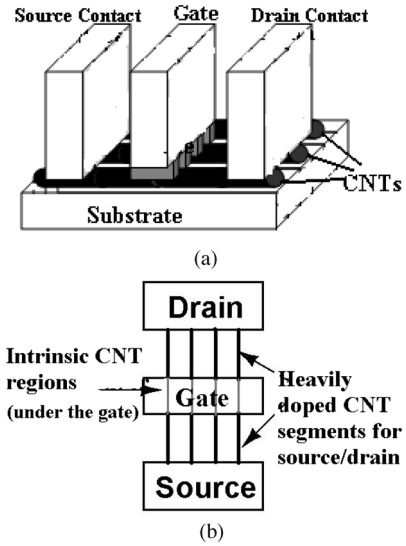


Fig. 1. Schematic diagram of a CNTFET. (a) Cross-sectional view. (b) Top view.

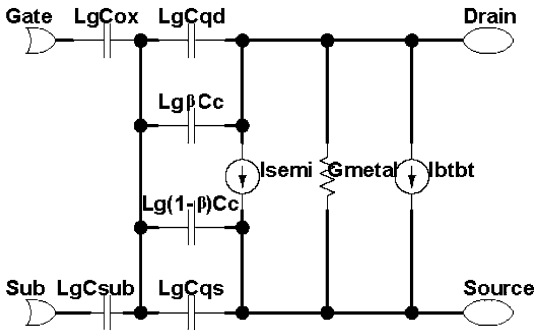


Fig. 2. Equivalent circuit model for the intrinsic channel region of a CNTFET [6].

represented by the integer pair (n, m) [6]. A simple method to determine whether a CNT is metallic or semiconducting is based on considering the indexes (n, m), i.e., the nanotube is metallic if $n = m$ or $n - m = 3i$, where i is an integer. Otherwise, the tube is semiconducting. The diameter of the CNT can be calculated from [6] as a function of m and n. Fig. 1 shows the schematic diagram of the CNTFET [6]. Similar to the silicon device, the CNTFET has four terminals. Also, a dielectric film is wrapped around a portion of the undoped semiconducting nanotube, and a metal gate surrounds the dielectric. Fig. 2 shows the equivalent circuit model implemented in HSPICE, as proposed in [6]. Heavily doped CNT segments are placed between the gate and the source/drain to allow for a low series resistance during the ON-state [8]. As the gate potential increases, the device is electrostatically turned on or off via the gate.

The I–V characteristics of the CNTFET are shown in Fig. 3, and they are similar to those of MOSFET. The CNTFET device current is saturated at higher $V_{\rm ds}$ (drain-to-source voltage) as channel length increases, as shown in Fig. 3, and the ON-current decreases due to energy quantization in the axial direction at 32 nm (or less) gate length [6]. The threshold voltage is defined as the voltage required to turn on the transistor, and the threshold

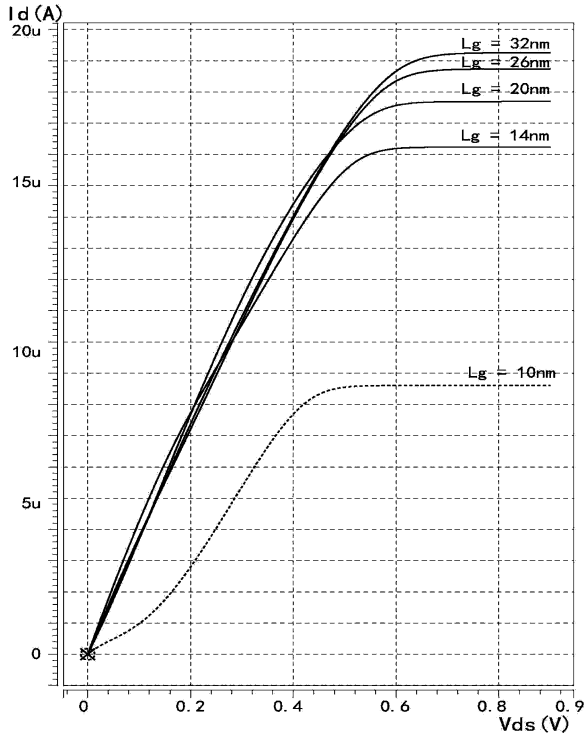


Fig. 3. I–V characteristics of a ballistic CNTFET.

voltage of the intrinsic CNT channel can be approximated to the first order as the half bandgap, which is an inverse function of the diameter [6]

$$V_{\rm th} \approx \frac{E_g}{2e} = \frac{\sqrt{3}}{3}\frac{aV_\pi}{eD_{\rm CNT}} \tag{1}$$

where $a = 2.49$ Å is the carbon-to-carbon atom distance, $V_\pi = 3.033$ eV is the carbon π–π bond energy in the tight bonding model, e is the unit electron charge, and $D_{\rm CNT}$ is the CNT diameter. Then, the threshold voltage of the CNTFETs using (19, 0) CNTs as channels is 0.289 V because $D_{\rm CNT}$ of a (19, 0) CNT is 1.49 nm. Simulation results have confirmed the correctness of this threshold voltage. As the chirality vector changes, the threshold voltage of the CNTFET will also change. The threshold voltage of the CNTFET is inversely proportional to the chirality vector of the CNT. For example, the threshold voltage of the CNTFET using (13, 0) CNTs is 0.423 V, while the threshold voltage of the CNTFET using (19, 0) is 0.289 V. Fig. 4 shows the threshold voltage of p-type CNTFET (PCNTFET) with CNTs of different chirality vectors. For n-type CNTFET (NCNTFET), the threshold voltage is determined similarly to that of the PCNTFET, but has an opposite sign [6]. The threshold voltage of the CNTFET depends only on the chirality vector of the CNT. Therefore, CNTFETs provide a unique opportunity for threshold voltage control by changing the diameter of the CNT [9]. Extensive research has been pursued for manufacturing well-controlled CNTs [10], [11]. In this paper, a dual-diameter CNTFET-based SRAM design is proposed and designed for best performance.

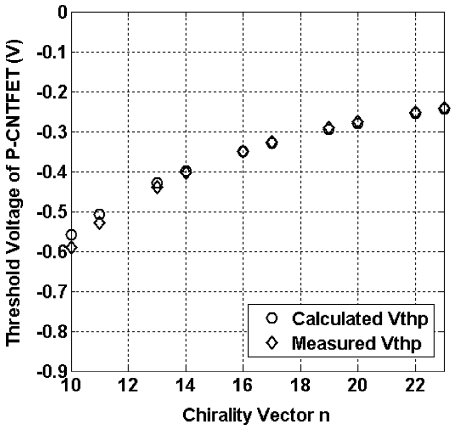


Fig. 4. Threshold voltage of PCNTFET with different chirality vectors.

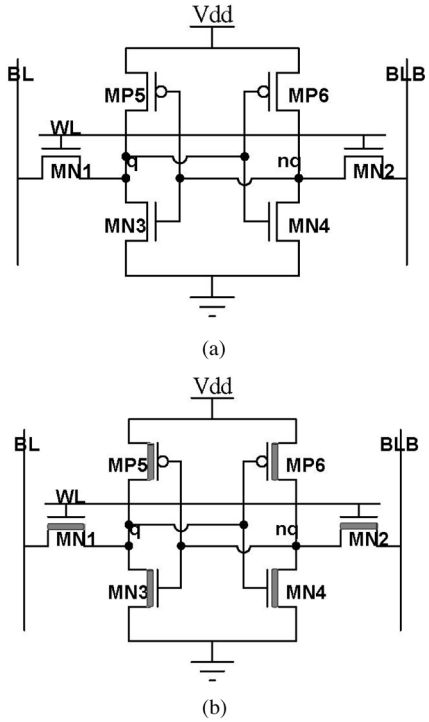


Fig. 5. 6T SRAM cell in (a) CMOS and (b) CNTFET.

III. SRAM Design

Fig. 5(a) shows the conventional [six-transistor (6T)] SRAM cell configuration used as the core storage element of most register file and cache designs in CMOS. With today's aggressive scaling, substantial problems such as power consumption and stability have already been encountered when the 6T SRAM cell configuration is utilized in CMOS at nanoscale ranges. In this paper, the 6T SRAM cell of Fig. 5(a) is designed using CNTFETs [shown in Fig. 5(b)], and its performance is assessed comprehensively with a newly proposed figure of merit, denoted as "SPR," to compare stability, power dissipation, and write time with other existing SRAM cell designs. The basic design concept of the CNTFET-based memory has been proposed in [13] by the same research group, and this paper presents the actual design of the concept addressing the realistic design challenges and issues such as performance, static noise margin (SNM), power consumption, and tolerance to process, power supply voltage, and temperature (PVT) variations.

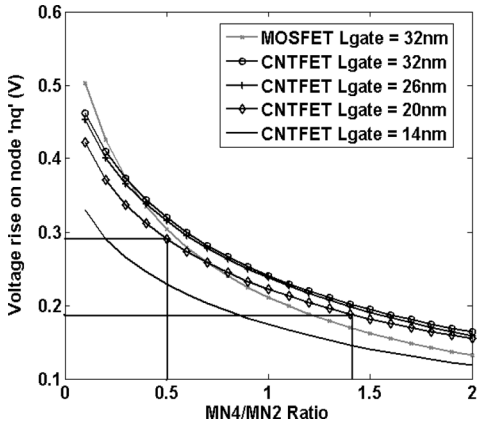


Fig. 6. MN4/MN2 ratio versus voltage rise at $\mathbf{nq}$ for SRAM cells.

A. Read Operation

Prior to the read operation, BL and BLB of Fig. 5(b) are precharged to high level. When the wordline signal WL is high, the access transistors MN1 and MN2 are turned on, and the data stored in the SRAM are read. However, a read-upset problem is present during the read operation, and this may change the data stored in the SRAM cell. The read-upset problem can be described as follows. Assume that the cell is currently storing 1 so that $\mathbf{q}$ is 1 and $\mathbf{nq}$ is 0. When WL is high, MN1 and MN2 are ON and the voltage at node $\mathbf{nq}$ will rise. An appropriate sizing ratio between MN4 and MN2 is required to limit the voltage at node $\mathbf{nq}$ to be lower than $V_{\rm th}$ such that the stored logic value does not change during the read operation. In the traditional CMOS design, the MN4/MN2 ratio should be greater than 1.28 for this requirement [12]. For the CNTFET SRAM design, simulations have been performed to establish the sizing ratio of MN4 and MN2. The gate and source of MN2 are connected to $V_{\rm dd}$, and the gate of MN4 is also connected to $V_{\rm dd}$ as the voltage at $\mathbf{q}$ needs to be set to 1. The simulation results are shown in Fig. 6 for various MN4/MN2 ratios and gate lengths. Unlike MOSFET, the transistor size ratio of the two CNTFETs is measured as the number of tubes in the two CNTFETs. As mentioned in Section II, the threshold voltage of the (19, 0) CNTFET is 0.289 V. Therefore, the MN4/MN2 ratio should be kept greater than 0.5 to keep the voltage of $\mathbf{nq}$ below threshold voltage. However, for fair comparisons, the MN4/MN2 ratio used in this paper for the CNTFET SRAM design needs to be greater than 1.4 to control the low state voltage below the threshold voltage of the 32-nm MOSFET, which is 0.18 V [16].

B. Write Operation

During the write operation, the wordline WL is high to allow the data on bitlines BL and BLB to be written into the SRAM cell. For a successful write to an SRAM cell, the pull-up transistor should not be too strong. Assume that the SRAM cell is

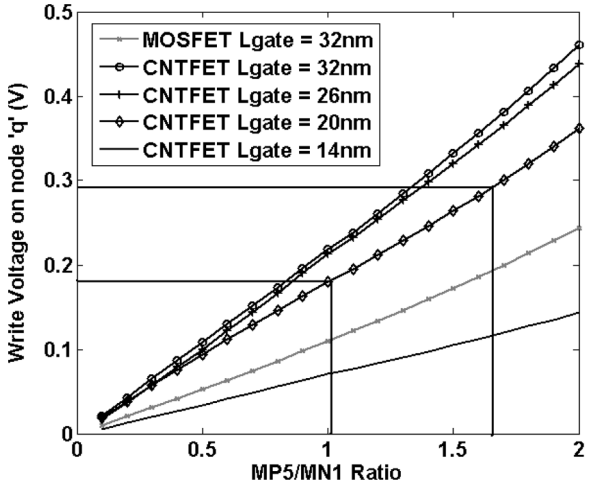


Fig. 7. MP5/MN1 ratio versus write voltage at **q** for SRAM cells.

storing "1" and it is required to write a new data "0" into the SRAM cell. The node **q** in Fig. 5(b) is going to be low, so the pass gate MN1 must be significantly more conductive than the PMOS MP5. In the traditional CMOS design, the MP5/MN1 ratio should not be greater than 1.6 [12]. For CNTFET SRAM design, simulations have been performed to establish the size ratio between MP5 and MN1. The bias voltage on the gate of MP5 is kept below $V_{\rm th}$, and the bias voltage on the gate of MN1 is $V_{\rm dd}$. Fig. 7 shows the simulation results for various ratios and channel lengths. Any MP5/MN1 ratio of less than 1.6 can pull node **q** below 0.289 V, which is the threshold voltage of a CNTFET with (19, 0) nanotubes. Similarly to the read operation, the MP5/MN1 ratio used in this paper for the CNTFET SRAM design needs to be less than 1 to ensure that the write voltage at node **q** is not higher than the threshold voltage of the 32-nm MOSFET (i.e., 0.18 V).

Therefore, for the proposed dual-diameter CNTFET-based SRAM cell design, the transistor size ratios among the pull-up FET, the pull-down FET, and the access transistors are MP5/MN1 $= 0.5$ and MN4/MN2 $= 1.5$. PCNTFETs with one tube are used for MP5 and MP6, while NCNTFETs with three tubes are used for MN3 and MN4. The number of tubes used for MN1 and MN2 is 2.

As the channel length of the CNTFET decreases to 32 nm or below, the drain current of the CNTFET decreases due to energy quantization in the axial direction. Phonon scattering in short-channel devices further reduces the ON-current [17]. As shown in Fig. 3, the drain current of CNTFET decreases dramatically when the channel length is less than 20 nm. Therefore, by considering area and performance, a 20 nm gate length is chosen in this paper for the design of the CNTFET-based SRAM cell.

As the distance between two adjacent tubes within the same device is 20 nm and the channel length chosen in this paper (as per previous discussion) is also 20 nm [6], the dimensions of the pull-up transistor MP5, the pull-down transistor MN3, and the pass-gate transistor MN1 are 40/20, 80/20, and 60/20 nm, respectively (40/20 nm denotes the width to length ratio). For a CMOS SRAM cell with a transistor length of 32 nm and circuit performance similar to the CNTFET SRAM cell proposed in this section, the widths of MP5, MN3, and MN1 are found to be 80, 160, and 120 nm, respectively. Therefore, there are two 80/32 nm PMOS transistors, two 160/32 nm NMOS transistors, and two 120/32 nm NMOS transistors in the CMOS SRAM cell. Compared to the CMOS at 32 nm feature size, the CNTFET-based SRAM cell has two 40/20 nm p-CNTFETs, two 80/20 nm n-CNTFETs, and two 60/20 nm n-CNTFETs. These transistors are used in the next section to establish the best operation under the optimized threshold voltages for the dual-diameter CNTFET-based SRAM cell.

IV. Dual-Chirality SRAM Cell Design

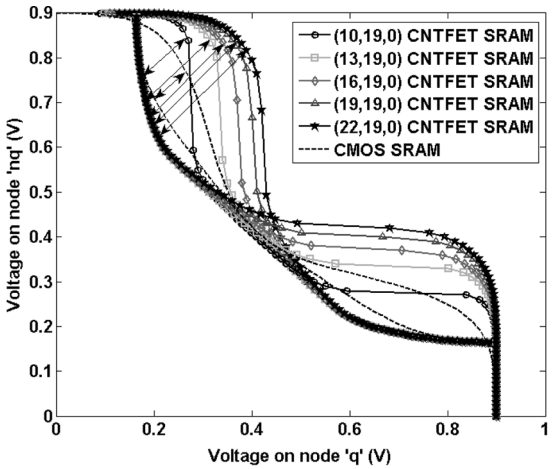
Since the threshold voltage of CNTFET can be controlled by adjusting tube's diameter, the design of CNTFET-based circuits with different threshold voltages is possible because CNTs can be grown with different diameters [9]–[11]. In this paper, NCNTFETs and PCNTFETs use CNTs that have different chirality vectors for the best (optimized) performance. However, all NCNTFETs use CNTs with the same chirality vector and all PCNTFETs also use the same chirality vector (the dual-diameter arrangement is used for simplicity, although additional threshold voltages could also be utilized by using CNTs with different diameters in the transistors).

A new index is defined for the CNTFET-based SRAM design, and it is given by the triplet (*np*, *nn*, m), where *np* and *nn* represent the first chirality vector "n" of the PCNTFETs and NCNTFETs, respectively, and m is the common second chirality vector "m" of the two CNTFETs. For example, an SRAM cell with (16, 0) PCNTFETs and (19, 0) NCNTFETs is represented by the index triplet (16, 19, 0). The difference in chirality between NCNTFETs and PCNTFETs must also take into account the performance of the SRAM memory cell. As for CMOS SRAM, the threshold voltage of the pull-up p-type FETs [MP5 and MP6 shown in Fig. 5(b)] have a close relationship with the SNM of the SRAM cell (the SNM is defined as the maximum value of dc noise voltage that can be tolerated by the SRAM cell without changing the stored bit [14]). The SNM is commonly used as a metric for static stability of an SRAM cell [15].

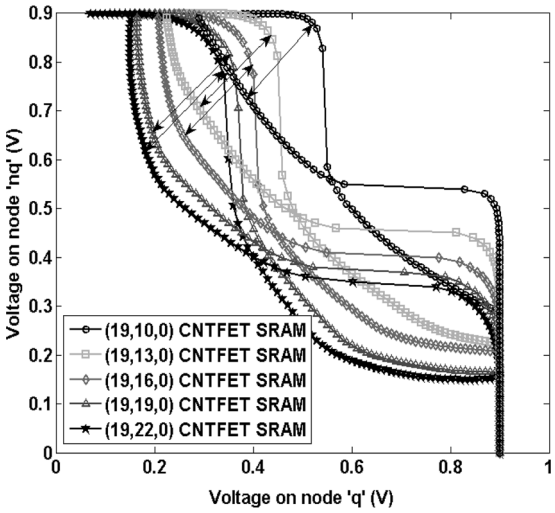
To investigate the SNM of the proposed dual-diameter CNTFET SRAM, extensive simulations have been performed on CNTFET SRAM cells with index triplets of (10, 19, 0), (13, 19, 0), (16, 19, 0), (19, 19, 0), and (22, 19, 0) for the transistors. Fig. 8 shows the simulation results of the read SNM of the SRAM cell at 0.9 V power supply and room temperature. For the 6T SRAM cell configuration in Fig. 5, the worst-case stability condition occurs when the cell is accessed for read operation, i.e., the read SNM is lower than the hold SNM. Simulation has shown that as the chirality vector of the PCNTFETs changes from (10, 0) to (22, 0), the SNM of the CNTFET SRAM is increased. As shown in Fig. 8(a), the read SNM of the CNTFET SRAM is larger than that of the CMOS SRAM at 32 nm feature size. Simulation has also been performed by changing the chirality vector of the NCNTFETs in the range from (10, 0) to (22, 0). As shown in Fig. 8(b), the values of the read SNM of

TABLE I
SNM AND WRITE TIME OF THE SRAM CELLS AT 0.9 V POWER SUPPLY AND ROOM TEMPERATURE

SRAM cell	Vth of N-type FET (mV)	Vth of P-type FET (mV)	SNM (mV)	Write time (ps)	SNM/Write Time (mV/ps)
(10, 19, 0) CNTFET SRAM cell	289	-550	125	20.51	6.09
(13, 19, 0) CNTFET SRAM cell	289	-422	175	23.45	7.46
(16, 19, 0) CNTFET SRAM cell	289	-343	206.3	24.97	8.26
(19, 19, 0) CNTFET SRAM cell	289	-289	244	29.70	8.21
(22, 19, 0) CNTFET SRAM cell	289	-250	262.5	32.25	8.13
32nm CMOS SRAM cell	180	-180	81.3	24.64	3.29



(a)



(b)

Fig. 8. SNM of the SRAM cell with (a) different PCNTFET chirality vectors and (b) different NCNTFET chirality vectors.

the CNTFET SRAM change little as the chirality vectors of the NCNTFETs change. Therefore, for best stability, the chirality vector of the PCNTFETs must be adjusted.

The stability of the SRAM cell can be increased by decreasing the absolute value of the threshold voltage of the pull-up transistor by controlling its chirality vector. However, there is a conflicting constraint between performance and stability. At a better ability to hold data, it is also harder to write new data into the SRAM cell, i.e., it takes more time to write new data. To find the optimum chirality for both PCNTFETs and NCNTFETs, both the SNM and the write time must be considered. Table I shows the SNM and the write time of the CNTFET SRAM cell with different threshold voltages of the PCNTFET at 0.9 V power supply and room temperature. Both the SNM and the write time increase with decrease of the absolute value of the threshold voltage of the pull-up transistor. For a highly stable and low-delay design, a high SNM and a fast write time are desired. Therefore, the SNM is divided by the write time to find the best threshold voltage of the PCNTFET for both high SNM and fast write time. As shown in Table I, when the threshold voltage of the PCNTFET is $|0.343\ \text{V}|$ for a (16, 19, 0) SRAM cell, the ratio between the SNM and the write time is the highest among the CNTFET SRAM cells listed in Table I. Therefore, the (16, 19, 0) SRAM cell is selected for best overall performance. It is also shown in Table I that the ratio between the SNM and the write time for the CNTFET SRAM cell is significantly higher than for the CMOS SRAM cell, i.e., high stability is attained at a low write time.

V. METRIC FOR MEMORY CELLS

To compare the dual-diameter CNTFET and CMOS SRAM cell configurations, a novel metric is introduced in this section. This is required to comprehensively assess the performance as a function of delay, stability with respect to noise, and power dissipation within a comprehensive metric. HSPICE simulations are performed using the Stanford CNTFET model [6] and the Berkeley Predictive 32 nm CMOS model [16] to compare the CNTFET and CMOS 6T SRAM cells. It has been shown in [15] that both the SNM and the static current noise margin (SINM) must be used to address the static stability of an SRAM cell. Therefore, SNM and SINM are multiplied together to yield a comprehensive figure of merit as the static power noise margin (SPNM). The power delay product (PDP) is an important parameter, and is often used to measure and compare the circuits. It has been shown in [17] and [18] that the CNTFET has very high ON/OFF current ratio compared to its CMOS counterpart. Therefore, the standby power of the CNTFET SRAM is

TABLE II
SPR OF SRAM CELLS AT 0.9 V POWER SUPPLY AND ROOM TEMPERATURE

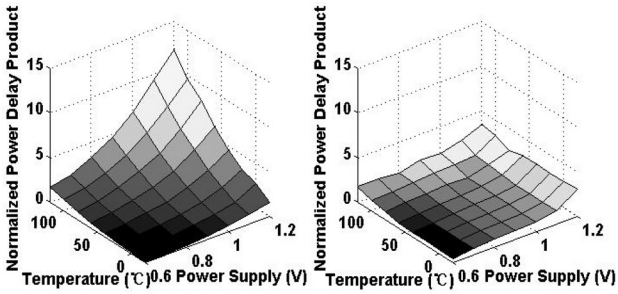
SRAM cell	SNM (mV)	SINM (uA)	Write Power (uW)	Write Delay (ps)	SPR (1/s)
CMOS SRAM cell	117.6	34.33	29.56	24.64	4.142e+9
CNTFET SRAM cell	206.3	31.53	16.47	24.97	1.582e+10

significantly lower than for the CMOS SRAM. However, it is also important to address write power dissipation as the power dissipated by a memory cell during the write operation is higher than the power dissipated during the read operation due to the full swing charge and discharge on the bitlines during the write operation. Therefore, the PDP of the SRAM cell proposed in this paper is the product of the write power and the write delay.

The new comprehensive performance metric that is proposed in this paper includes delay, stability, and power. It is given by dividing the SPNM by the PDP, and this is referred to as the SPNM to PDP ratio (SPR). The SPR (in seconds inverse) can be expressed as SPR = (SNM × SINM)/(Write Power × Write Delay) and provides a metric for high stability, low delay, and low power in the operation of a memory cell. SPR is also versatile as it can be used to assess performance under different operational conditions, such as standby and write. Table II shows the SNM, SINM, Write Power, and Write Delay of the CMOS SRAM cell and the CNTFET SRAM cell at 0.9 V power supply and room temperature. As shown in Table II, the CNTFET SRAM cell is designed to have the same write delay as the CMOS SRAM cell. However, the other figures of merit may change to meet this requirement. The decrease of the write delay implies that it is easier to write data into an SRAM cell, thus making stability degrade. Also, the improvement in delay performance usually requires a larger transistor size, thus increasing power consumption. Therefore, to comprehensively assess performance as a function of delay and stability with respect to noise and power dissipation, a new metric must be used. The proposed SPR provides such a metric for an SRAM cell in terms of delay, stability, and power. Table II confirms that the SPR of the CNTFET 6T SRAM cell is four times higher than its CMOS counterpart, hence attaining low power, high stability, and low delay within the comprehensive metric provided by the SPR under write conditions.

VI. IMPACT OF VARIATIONS

Systematic and random variations in PVT pose a major challenge to nanoscale CMOS integrated circuits. Systematic variations in power supply voltage and temperature are shared among all devices and have become a significant concern to the parametric yield in terms of energy and delay. Fig. 9 shows the PDP with different supply voltages and temperatures for the CNTFET and CMOS cells. All simulation results are normalized to the PDP at 0.9 V power supply and room temperature. Due to the ballistic transport of the CNTFET, the PDP variation of the CNTFET to voltage and temperature variations is very



(a) (b)

Fig. 9. PDP of CMOS. (a) CNTFET. (b) SRAM cells versus power supply and temperature variations.

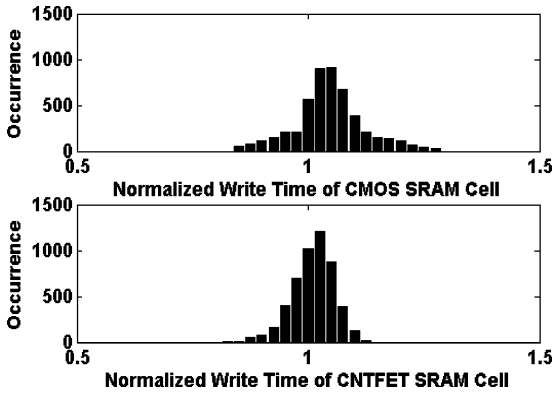


Fig. 10. Write time distribution of CMOS and CNTFET SRAM cells.

small. Therefore, the CNTFET is very insensitive to voltage and temperature as systematic variations.

In CMOS process, random process variations often cause geometric variations in the gate (length, width, and thickness) as well as gate oxide thickness. In short-channel devices, a variation in channel length also induces a change in threshold voltage due to the drain-induced barrier lowering [19]. These variations still exist even in CNTFET. However, due to the cylindrical geometry, a variation in the gate oxide thickness that strongly affects the drive current and capacitance of CMOS transistors has a negligible impact on the CNTFET's operation. The gate width in CNTFET is not the effective channel width of the transistor. This depends only on the CNT diameter and the number of tubes under the gate, and does not affect the drive current. As in [20], only the CNT diameter has the strongest impact on the CNTFET performance, while other process variations have only a small impact. Monte Carlo simulation by HSPICE has been performed to investigate the impact of the random variations on the delay and power of the CNTFET, and CMOS SRAM cells at 0.9 V power supply and room temperature. Fig. 10 shows the distribution of the write time of the CNTFET and CMOS 6T SRAM cells under geometric parameters with random changes. All simulation results are normalized to the SRAM's write time under no process variation. Fig. 10 shows that the write time of the proposed dual-diameter CNTFET 6T SRAM cell has much better tolerance to process variations compared to its CMOS counterpart. Fig. 11 shows the distribution of the standby power

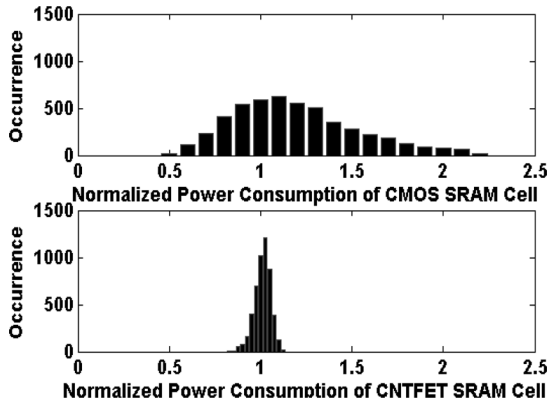


Fig. 11. Standby power dissipation distribution of CMOS and CNTFET SRAM cells.

consumption of the CNTFET and CMOS 6T SRAM cells. As in the previous cases, all simulated results are normalized to the SRAM cell standby power consumption under no process variation. Due to the significantly low standby power consumption and fewer parameters causing changes in power consumption, the CNTFET SRAM cell shows a significantly better tolerance to process variations.

VII. Conclusion

This paper has investigated the use of CNTFETs in 6T SRAM design. As the threshold voltage of the CNTFET can be controlled easily by changing the chirality vector of the CNTs, a dual-diameter CNTFET SRAM cell configuration with different threshold voltages is designed, which is made possible by using different diameters for the p-type and n-type CNTs in the cell. The best chirality for the PCNTFETs was selected to achieve high stability, fast write time, and low power consumption. The proposed design shows significant improvements (compared to the design of [7]) in terms of power consumption and area.

A new comprehensive metric for SRAM cells denoted as SPR has been proposed in this paper. SPR is a composite and versatile performance measure in terms of stability, power, and delay. The proposed dual-diameter CNTFET SRAM cell has a better SPR under write operation than its CMOS counterpart cell. Moreover, simulation has shown that the proposed dual-diameter CNTFET-based SRAM design has significant lower sensitivity to PVT variations.

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