Integrated Bias Circuits of RF CMOS Cascode Power Amplifier for Linearity Enhancement

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***Abstract*—This paper presents a highly linear differential cascode CMOS power amplifier (PA) with gate bias circuits in Common Source (CS) and Common Gate (CG) amplifiers. The proposed Class-D bias circuit at the gate of a CS amplifier injects a reshaped envelope signal only when the envelope signal is above a certain threshold voltage. This improves the linearity of the PA without significantly degrading the efficiency in a high-power region. In addition, the proposed bias circuit at the gate of a CG amplifier controls the second-order nonlinear components to improve the linearity and to reduce the sideband (IMD or ACLR) asymmetry, simultaneously. A single-stage PA including the bias circuits was fabricated using a 0.18-μm CMOS process, with an integrated passive device (IPD) transmission line transformer (TLT). With a 3.5 V supply, the measurements show that 26.8 dBm with 43.3% PAE at −37 dBc ACLR (5 MHz offset) and 27.8 dBm with 45.8% PAE at −33 dBc ACLR (5 MHz offset) at 1.85 GHz under 3GPP WCDMA test without digital pre-distortions.**

***Index Terms*—ACLR, ACLR asymmetry, baseband injection, baseband mismatch, bias circuit, bias network, Class-AB, cascode amplifiers, CMOS, differential, envelope injection, IMD, IMD asymmetry, IPD, linear amplifier, linearity, linearization, power amplifier (PA), transmission line transformer (TLT), WCDMA.**

I. Introduction

DESIGNING a CMOS RF power amplifier (PA) is very challenging, particularly when implementing a single chip radio transceiver that provides low cost and high integration in handheld applications [1]–[10]. However, the low breakdown voltage of a CMOS device and no substrate via hole to the ground make it difficult to implement a watt-level CMOS PA. To overcome these problems, a differential cascode structure PA using a transmission line transformer (TLT) is widely used in high efficiency CMOS PAs [1]–[7]. However, linear PAs that amplify non-constant envelope signals efficiently remain problematic when implemented with CMOS. Thus, many studies have focused on overcoming the disadvantages of CMOS by adjusting the gate bias, as described in [11]–[13], because the performances of the PAs are strongly determined by their gate bias [11]–[16].

These previous works demonstrated that adaptive bias control allows highly efficient and linear PAs, especially in handheld terminals [14]. This makes the gate bias follow the average input power level. When a high voltage envelope signal enters the PA, the gate bias is increased from low to high (close to Class-A). This improves the linearity at the expense of current consumption. It improves the efficiency only in large back-off regions, but it does not improve both the efficiency and linearity in high-power regions.

To enhance the linearity in an amplifier, an envelope signal injection scheme was introduced theoretically and experimentally in previous researches [17]–[19]. The injected envelope signal reduced the intermodulation distortion (IMD) components by canceling the distortions. Previous works, which were difficult to estimate the proper amplitude and shape of the injecting signal, used an additional VGA and phase shifter prior to the PA on a printed circuit board (PCB) to make an appropriate envelope signal to improve the linearity of the PA experimentally [18] and [19]. Due to the large implementation sizes, these were adopted in base station PAs, but they are not suitable for handheld PAs. However, a CMOS PA can easily be integrated with bias control circuits, thus improving its linearity. A previous study showed that the envelope signal injection with an integrated bias circuit improves the linearity of the amplifier [17]. However, this was applied to a small signal amplifier, VGA in the transmitter, to enhance the linearity.

Envelope injection through a bias circuit is a possible solution in CMOS linear PAs, but it is difficult to make the bias circuit function as a proper envelop shaper. The previous research [17] shows that some injected envelope signals degrade the linearity even in a small signal amplifier. Thus, careful considerations are necessary to have proper envelope signal injections. Furthermore, the gate capacitance of a CMOS power transistor is as large as 20 pF for watt-level power, which become a part of the load of an integrated bias circuit. The shape and amplitude of the injection signal are key factors to secure the good linearity in a PA. However, there has been no research on a linear PA with integrated bias circuits to inject an envelope signal. If the distorted envelope signal, due to the slower change of the gate bias circuit's output signal compared to the incoming envelope signal, enters the PA, it will generate additional distortions and degrade the linearity. This happens with conventional adaptive bias circuits, as the large gate capacitances of the power transistors are mostly neglected. Therefore, we propose an integrated Class-D bias circuit to have a properly reshaped envelope signal injection. This allows a PA to have linear amplification in

Manuscript received May 17, 2011; revised November 01, 2011; accepted November 08, 2011. Date of publication January 06, 2012; date of current version February 03, 2012. This work was supported by the National Research Foundation of Korea Grant funded by the Korean Government (No.2011-006556).

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Digital Object Identifier 10.1109/TMTT.2011.2177857

a high-power region without degrading the efficiency. The gate bias voltage is increased according to the incoming envelope signal only when the envelope signal is above a certain threshold voltage. It remains at the fixed voltage, the initial operating bias, when the envelope voltage is less than the threshold voltage.

Additionally, because the asymmetry between the upper and lower sidebands in a PA determines the linearity of the PA [20]–[28], reducing it is important. Asymmetry in sideband components complicates digital pre-distortion implementations due to the different compensation requirements for lower and upper sidebands. The bias circuit for the envelope signal injection also experiences the sideband asymmetry problem in small signal amplifiers [17]. Therefore, in this paper, the bias circuit of a CG amplifier in a cascode structure is studied to reduce the sideband asymmetry by controlling second-order nonlinear components at an envelope frequency (Δf) and a second-harmonic $(2f_0)$ [20]–[26]. Furthermore, an improvement in the linearity near the maximum linear power is also achieved by controlling the impedance at $2f_0$.

This paper is organized as follows. In Section II, the reshaped envelope signal injection with the Class-D bias circuit of the CS amplifier in the cascade structure is introduced. It contains a model of the proposed injection signal for a CMOS PA. The reduction of the sideband asymmetry and the IMD3 components by the bias circuit of the CG amplifier in the cascade structure are described in Section III. In Section IV, the implementation and measurement results are presented. The PA was also tested with modulated input signals, meeting the linearity and output power requirements of WCDMA standards. We design a single-stage PA fabricated using a 0.18-μm CMOS process with IPD TLT. To the best of the author's knowledge, it shows the highest efficiency and linearity reported for WCDMA CMOS PAs so far, and these are comparable to those of GaAs-based PAs.

II. Linearization With Reshaped Envelope Signal Injection and Thresholding Using a Class-D Bias Circuit

In this section, the principle of the improvement of the linearity without a significant reduction of the efficiency when the power approaches high levels, due to reshaped envelope signal injection, at the gate of the CS amplifier in the cascade structure is explained. To explain this concept easily, the PA's output envelope is shown in Fig. 1. This figure shows the reshaped envelope injection signal proper for a CMOS PA to enhance the linearity and efficiency while amplifying the modulating signal ($\Delta f = 5$ MHz). Since a two-tone signal has a time-varying envelope, it causes the PA to operate not only in weakly nonlinear regions but also in strongly nonlinear regions. Thus, the PA's gain is degraded near the peak power [29]. This makes the output top-compressed, as shown in Fig. 1(a). This figure shows only the gain compression of the PA, but phase distortion also exists in strongly nonlinear regions. It increases the out-of-band components, such as the IMDs [29].

Thus, we adopt the envelope signal injection to CMOS PA to improve the linearity. However, there are several considerations to make a proper injection signal. The distorted PA's output due to the injection of the distorted envelope signal is also illustrated

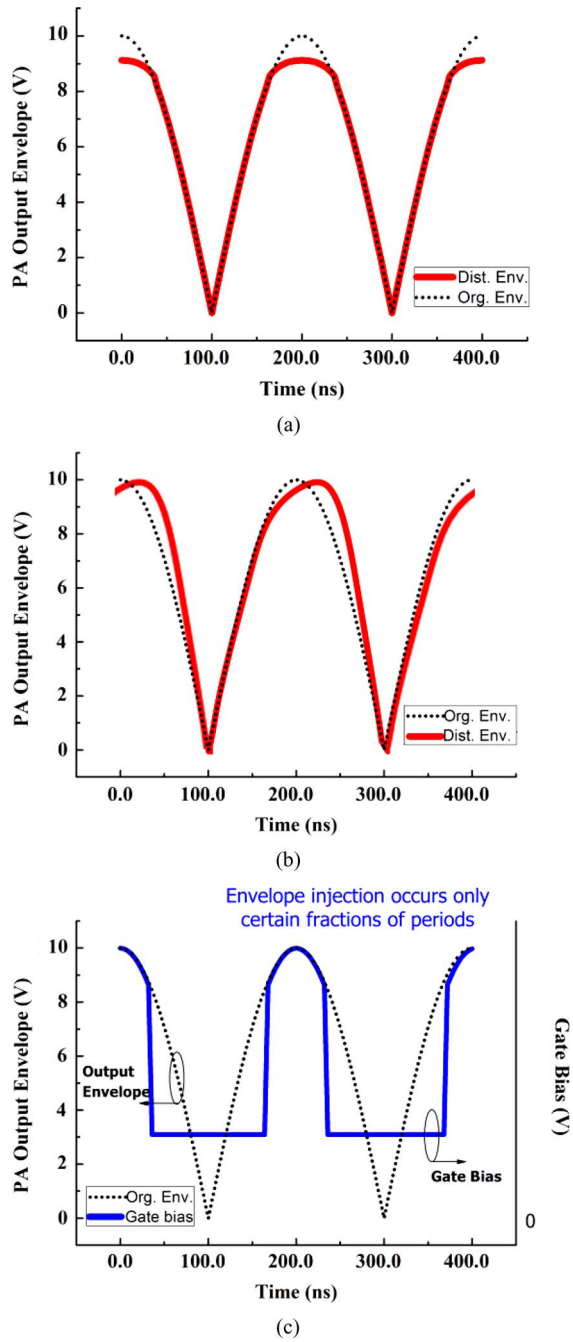


Fig. 1. Principle of the proposed reshaped envelope signal injection for linearity and efficiency enhancement. Original envelope signal and distorted envelope signal at high power due to (a) gain compression of the PA, and (b) wrong injection. (c) Conceptual gate voltage waveform of the reshaped envelope signal injection.

in Fig. 1(b). The major source of the distortion in this scheme, due to the injection signal, is expected to be the large gate capacitances of the power transistors which increase the charge or discharge time of the bias circuit. This will generate much more severe distortions when it handles a higher output power or higher data rate. To overcome this problem, we proposed reshaping the injecting envelope signal with a Class-D bias circuit. This reduces the gain and phase distortions of a PA by increasing the gate bias only when the envelope signal is above a certain

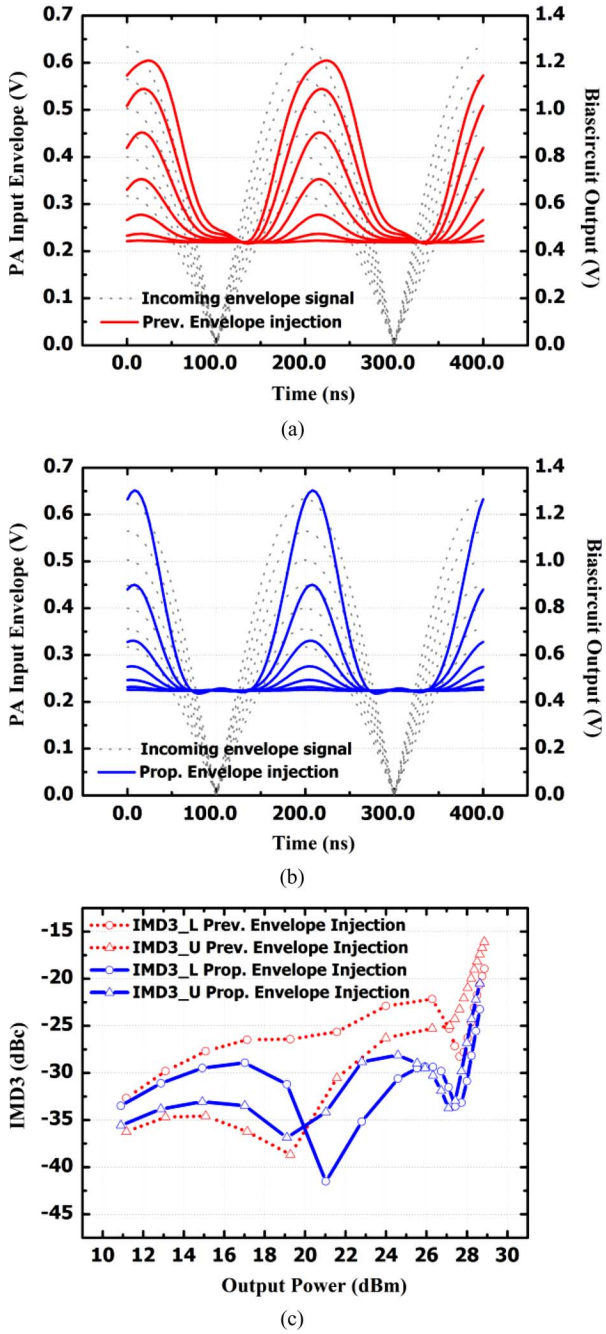


Fig. 2. Two-tone simulation results ($\Delta f = 5$ MHz). Simulated injection signals with (a) previous bias circuit and (b) proposed bias circuit for incoming envelope signals. (c) Simulated IMD3s with different bias circuits.

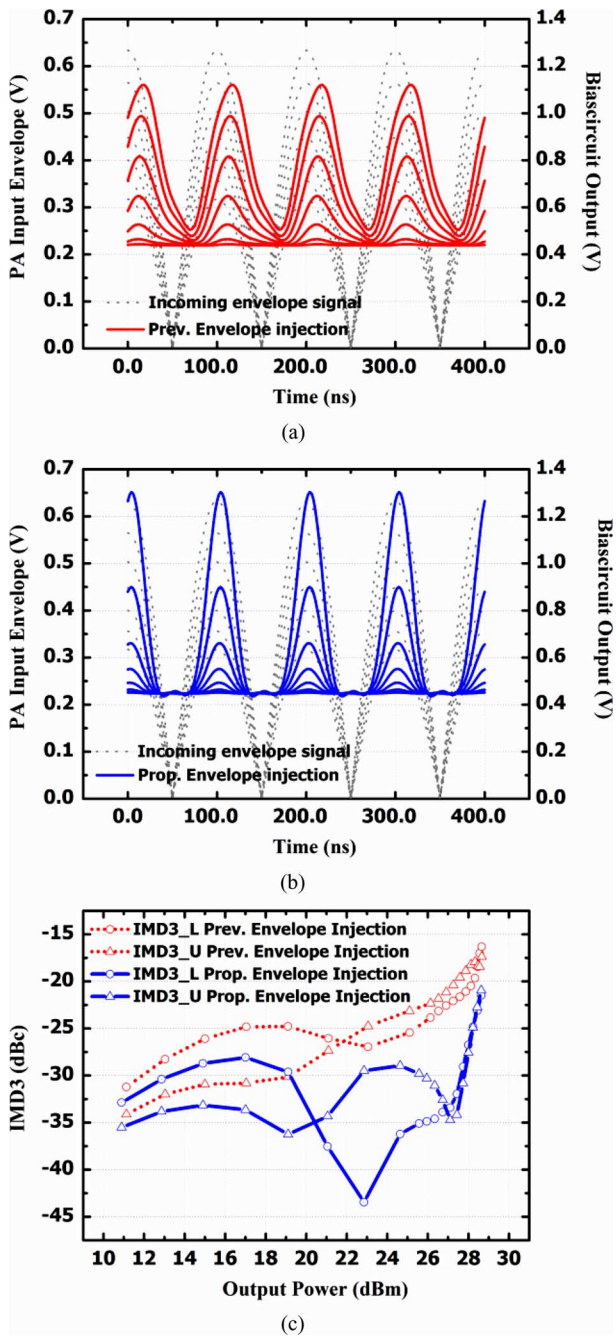


Fig. 3. Two-tone simulation results ($\Delta f = 10$ MHz). Simulated injection signals with (a) previous bias circuit and (b) proposed bias circuit for incoming envelope signals. (c) Simulated IMD3s with different bias circuits.

threshold voltage, as shown in Fig. 1(c). Thus, the current handling burden of the integrated bias circuit is also reduced considerably.

A. The Proposed Class-D Bias Circuit at the CS Amplifier

To show that the distorted output of the bias circuit degrades the linearity of the PA's output directly, we compare the two-tone simulation results with the two different bias circuits. The time domain waveforms of the two-tone simulation and the IMD3s for different values of Δf (5 and 10 MHz) are shown in Figs. 2 and 3. Existing bias circuits [11]–[14] are designed to increase the gate bias by the average input power level; when using them, it is not necessary to discharge as fast as the incoming envelope signal. Thus, existing circuits cannot inject the proper envelope signal to the gate of a CMOS PA. The distorted gate bias at transition regions near 100 ns in the discharge region in Figs. 2(a) and 3(a) generates additional nonlinearities in the PA. These results show that the distorted, in terms of the magnitude and phase, injection signal degrades the linearity of a PA. This distortion is expected to be more serious in future communication applications, which require the wider modulation bandwidths for the higher data rates. Therefore, a reshaped envelope signal injection with a

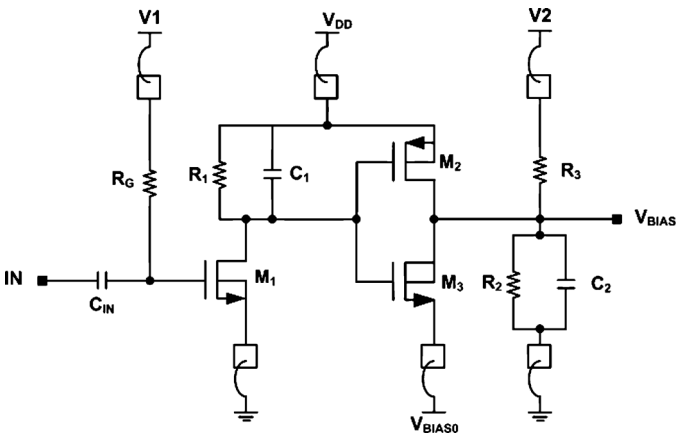


Fig. 4. Schematic of the proposed bias circuit for the reshaped envelope signal injection.

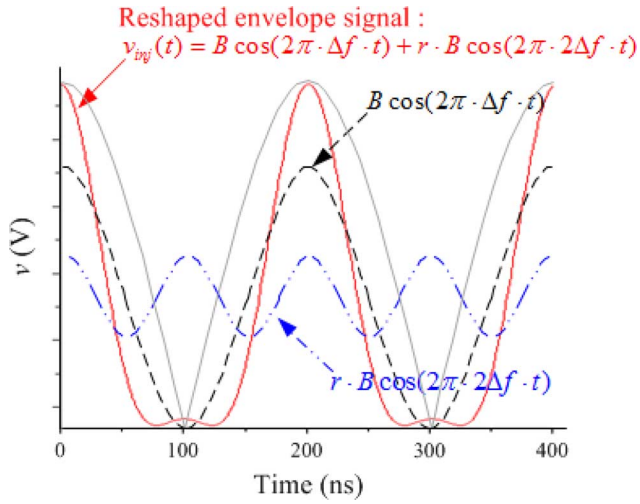


Fig. 5. Representation of the proposed injection signal with Δf and 2Δf components when $r = 0.33$.

threshold is proposed. This implies that the bias circuit for the proper envelope signal injection to the PA require an additional fast pull down network to reshape the envelope, which is a key difference from previous bias circuits [11]–[14]. The simulated IMD3s in Figs. 2(c) and 3(c) show sideband asymmetry, but this will be discussed in the next section.

Fig. 4 shows a schematic of the proposed bias circuit with a Class-D envelope amplifier, which is used to generate the proposed injecting signal, as shown in Figs. 2(b) and 3(b). The schematic is similar to the previous adaptive bias circuit [11]–[13], but it has an additional discharge current path consisting of an nMOS transistor (M_3) for the reshaped envelope signal injection. The proposed bias circuit consists of two parts: the envelope detector of the input signal that uses an nMOS transistor (M_1) with an R-C network, and an envelope amplifier. When an increasing voltage envelope signal enters the input of the bias circuit, the output voltage of the first stage decreases from V_{DD} to a lower value, and the pMOS (M_2) transistor then begins to charge the output node from the initial value (V_{BIAS0}) to a higher value. When the input envelope signal decreases, the V_{BIAS} is decreased to V_{BIAS0} at the output. The pull-down network of the bias circuit studied in earlier papers [11]–[13] consisted of only an R-C network. However, in this work, the additional discharge path of the nMOS (M_3) is introduced to inject the reshaped envelope signal to reduce the additional distortion caused by the injection signal.

Because the gate bias of the first stage in the bias circuit is not a subthreshold bias but is 0.7 V, it amplifies all of the envelope signals. In addition, the injection angle and the shape of the injection signal are determined by the size ratio of pMOS (M_2) and nMOS (M_3) in the second stage. The size of the pMOS (M_2) transistor is eight times larger than that of the nMOS (M_3) transistor, thus providing the bias circuit with stronger pull-up than pull-down network, which is important in obtaining high linearity of a linear PA to increase the voltage for large envelope signals. Because the total width of the transistor in the bias circuit is much smaller than that of the PA, there is no degradation in the overall efficiency. To implement the gate bias circuit in the power stage, there has to be the additional consideration of putting the gate bias at the upper limit. If the gate bias exceeds the upper limit, serious degradations of the efficiency and reliability of the PA will arise. To implement the limiting circuit, the uncommon body connection is used to make a p-n junction diode in the nMOS (M_3) between the body and the source without additional circuits. This connection of the drain and body also assists reducing the discharge time of the Class-D envelope amplifier due to the body effect.

B. The Model of the Proposed Envelope Injection Signal

In previous researches [17]–[19], linearities are improved due to injection envelope signals. Preceding PA studies [18], [19] noted that the 'proper' choice of the amplitude and phase increased the linearity. We neglect the phase difference between the incoming envelope signal and the injecting signal to consider only the gain degradation of the PA for a large incoming envelope signal. We then define the optimum amplitude of the injecting signal with the Class-D bias circuit. The simulated output of the proposed Class-D bias circuit at the gate of the CS amplifier is shown in Fig. 2(b). This is reshaped by the combination of Δf and 2Δf [30], as in Fig. 5, with the incoming envelope signal. This is possible due to the Class-D output stage of the bias circuit. The output signal of the bias circuit has many harmonics of Δf, which is the fundamental frequency of the inverter input signal from the rectifying stage in the bias circuit. Thus, the following expression is used to model the proposed injection signal, whose expression has an additional term for reshaping the injection signal. This is the difference comparing with the previous research [17]–[19]

$$v_{\mathrm{inj}}(t) = B\cos(2\pi\cdot\Delta f\cdot t) + r\cdot B\cos(2\pi\cdot 2\Delta f\cdot t). \quad (1)$$

Here, B is the amplitude of the proposed reshaped envelope injection signal, which is determined by the input envelope signal and the gain of the bias circuit. The gate bias of M_1 and the resistor (R_1) in the first stage of the bias circuit in Fig. 4 are important to generate the proper amplitude of the injection signal. It should be noted that the injection angle does not change and that the amplitude of the injection signal changes

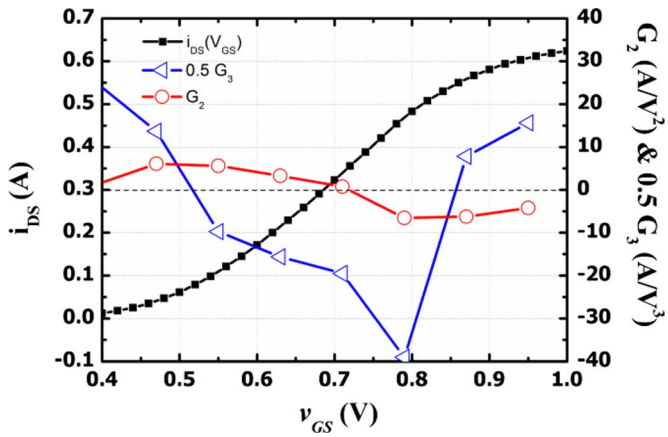


Fig. 6. Large signal transfer curve of CMOS PA which is used in this work.

with the Class-D bias circuit for various incoming envelope signals. The constant r is the second harmonic injection ratio (2Δf component to Δf one), which determines the shape of the injection signal. We choose an r value of 0.33 from the simulation result in this work. The proposed injection signal with $r = 0.33$ is shown in Fig. 5.

C. Analysis of the Proposed Linearization

Because previous envelope signal injection studies in PA [18], [19] include no investigation with a behavioral model of a designed PA, there must be a limitation in the choice of amplitude, which is important to integrate a bias circuit with a PA. To find the amplitude of the envelope injection signal, the characteristics of CMOS PAs are analyzed using the large signal *I–V* analyses that were introduced in earlier studies [31]–[33]. The amplitude of the injecting signal was found to compensate the nonlinearities. This is explained via the equations shown below. If the input voltage consists of two-tones that have the same amplitude of A, the following expression is used to include the injection signal. The expression is given by [17]–[19]

$$\begin{aligned} v_{\rm GS}(t) &= V_{\rm GS} + v_{\rm gs}(t) \\ &= V_{\rm GS} + A\cos(2\pi \cdot f_1 \cdot t) + A\cos(2\pi \cdot f_2 \cdot t) \\ &\quad + B\cos(2\pi \cdot \Delta f \cdot t) + r \cdot B\cos(2\pi \cdot 2\Delta f \cdot t). \end{aligned} \tag{2}$$

Here, f_1 is the frequency of the lower tone, f_2 is the frequency of the upper tone, $V_{\rm GS}$ is the DC gate bias voltage, and $v_{\rm gs}$(t) is an AC signal, including a two-tone signal and the proposed injection signal. This is different from previous works [17]–[19] in that the phase term of the injection signal is neglected and the r and 2Δf terms are introduced, as mentioned earlier.

The transfer function of the PA is shown in Fig. 6 when it operates at 0.7 V with the optimum load line. The major difference compared to the small signal transfer function is that the drain current is reduced at the high input signal in large signal regimes [31]–[33]. Assume that the drain current of the PA with respect to its input can be expanded in a Taylor series in large signal regimes [31]–[33], which is given by

$$\begin{aligned} i_{\rm DS}(V_{\rm GS} + v_{\rm gs}) &= i_{\rm DS}(V_{\rm GS}) \\ &\quad + G_1 \cdot v_{\rm gs} + G_2 \cdot v_{\rm gs}^2 + G_3 \cdot v_{\rm gs}^3 + \cdots. \end{aligned} \tag{3}$$

The resultant coefficients G_n are shown versus $v_{\rm GS}$ in Fig. 6. The coefficients are defined by

$$G_n = \frac{1}{n!} \cdot \left. \frac{\partial^n i_{\rm DS}[v_{\rm GS}]}{\partial v_{\rm GS}^n} \right|_{v_{\rm GS}=V_{\rm GS}} \tag{4}$$

in [31], and piecewise linear approximation of G_2 and G_3 is used in [33]. In this case, G_2 and G_3 have negative and positive values with a large input signal above 0.86 V, as in Fig. 6. The other higher order nonlinear terms in (3) are ignored for a simple analysis [17] and [18]. By inserting (2) into (3), the upper IMD3 component at $2f_2 - f_1$ of the drain current is then given by the following equation:

$$\begin{aligned} &i_{{\rm DS},3U}(v_{\rm GS}) \\ &\quad = i_{{\rm DS,int}.3U} + i_{{\rm DS,inj}.3U} \\ &\quad = \frac{3}{4}G_3A^3 + \frac{3}{4}G_3AB^2(1+2r) + G_2AB(1+r). \end{aligned} \tag{5}$$

When G_3 is positive, $i_{{\rm DS},3U}$ increases with A^3. Thus, this becomes significant at a large input signal. In other words, when $v_{\rm GS}$ is larger than 0.86 V, the current slope decreases as in Fig. 6 and AM-AM distortion occurs. This degrades the PA's linearity upon large input signals. The first term in (5) always exists in the IMD3 component, the intrinsic nonlinear component, which is independent of the injecting envelope signal. However, the second and third terms in (5) are generated by the envelope injection. Therefore, these terms can reduce the IMD3 with the 'proper' selection of B. Thus, far, there are no differences compared to previous analyses [17]–[19] except that r and 2Δf terms are introduced for shaping the injection signal. We can extract the non-linear coefficient of the designed PA in large signal regimes so that we can determine the amplitude of the injecting envelope signal to compensate the intrinsic IMD3. The first term is a positive constant judging from the graph in Fig. 6. The minimum $i_{{\rm DS},3U}$ exists when its derivative with respect to B is zero. Thus, the resultant $B_{{\rm MIN}(i_{{\rm DS},3U})}$ for the minimum $i_{{\rm DS},3U}$ is as follows:

$$B_{{\rm MIN}(i_{{\rm DS},3U})} = -\frac{2G_2}{3G_3} \cdot \frac{1+r}{1+2r}. \tag{6}$$

When $B_{{\rm MIN}(i_{{\rm DS},3U})}$ is 0.22 V considering $r = 0.33$ from Fig. 5, $G_2 \approx -6.3$ and $0.5 \cdot G_3 \approx 7.8$ from Fig. 6 at $v_{\rm GS} = 0.86$ V. This indicates that the proposed injection signal's swing from 0.48 V to 0.92 V improves the linearity of the PA, whose operating bias point is 0.7 V. The additional fine tuning of the reshaped envelope injection signal is performed to change the output impedance by controlling the gain of the overall envelope amplifier using the gate bias of the first stage.

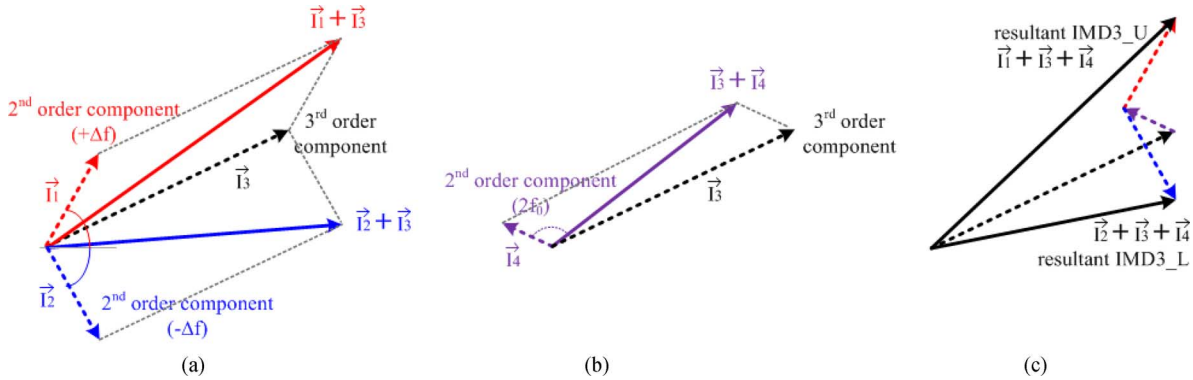


Fig. 7. Vector representation of the IMD3 components. (a) IMD3 components after adding the terms generated from the second-order nonlinear components at Δf. (b) $2f_0$. (c) Resultant upper and lower IMD3 components.

III. Linearization With Controlling the Impedance for Second-Order Nonlinear Components

Because of disadvantages of CMOS, such as no substrate via-hole in the process and its low breakdown voltage, the differential cascode structure is widely used to implement a watt-level CMOS PA [2]–[7]. Many differential cascode CMOS amplifiers use a large biasing resistor at the gate of the CG amplifier [2]–[7]. The connection of the gates in the differential CG amplifier creates a virtual ground at the fundamental frequency, but it has a high impedance value at Δf due to large bias resistor. This may be fine for a switching PA or a small signal amplifier. However, we find that the gate bias circuit of the CG amplifier directly effects the PA's linearity i.e., both the asymmetry and the magnitude of the IMD3, in a differential cascode PA. Additionally, the linearity of the CG amplifier (second stage) is more important than that of the CS amplifier (first stage) for the overall linearity [34]. In this section, the gate bias circuit of a CG amplifier in a differential cascode PA is studied to reduce the sideband asymmetry and to enhance the linearity near the maximum linear power.

A. IMD3 Asymmetry Sources in PA

IMD3 asymmetry is one of the key factors in determining the PA's linearity. Therefore, a considerable amount of efforts has been made to understand the mechanism of the IMD3 asymmetry of a PA experimentally and theoretically [20]–[28]. We can make the following two conclusions from the previous works.

1) A lower gate bias voltage generates the greater IMD3 asymmetry. The large signal IMD characteristics with various gate biases in a CS PA were studied in [32]. To create a null in the IMD in a high-power region, the PA has to be biased close to Class-B; it becomes more linear than that close to Class-A, especially in a high power region. Thus, the gate bias of the CG amplifier in a cascode amplifier must be close to Class-B. However, this operating bias point also introduces IMD asymmetry problems. Bias dependence of IMD asymmetry was reported in [27] and [28].
2) Second-order nonlinear components related to IMD3 asymmetry. While intrinsic IMD3s are generated by the third-order nonlinearity of an amplifier, additional IMD3 occurs due to the mixing of fundamental frequency components with second-order nonlinear components (Δf and $2f_0$) [22]–[26]. Because the asymmetry in IMD3s can be represented as vector sum in Fig. 7 [25], the opposite phase between Δf and $-\Delta f$ due to imaginary impedance at Δf creates a difference in the magnitude and phase in the lower and upper IMD3 [20] and [25]. The Δf component contributes to IMD3 asymmetry much more than the $2f_0$ component [26], and the $2f_0$ component contributes to the magnitude of the IMD3 as in Fig. 7. Thus, the impedance with the bias circuit at $2f_0$ is tailored very carefully.

B. Impedances of a Bias Circuit in a Differential Cascode PA

To observe the sources of IMD3 asymmetry in a differential cascode PA, we analyzed the imaginary parts of the load and source impedances of the PA over various frequency ranges from DC to 1 GHz as shown in Fig. 8(a). Output and input BALUNs are used in the differential PA for matching as well as combining and dividing. These allow virtual grounds at the centers of the primary coils in the BALUNs at the fundamental frequency and odd harmonics. It simultaneously sums up the even harmonics, including Δf. However, the simulated imaginary impedances are less than 1 Ω up to 160 MHz at both the load and the source, as the center tap is directly connected to the low impedance at the low frequency to apply the bias. Therefore, there are no sources of IMD3 asymmetry in an input and output matching network due to the use of a bias circuit with the BALUN in a differential PA.

However, IMD3 asymmetry exists, as shown in Figs. 2(c) and 3(c). We found that the additional IMD3 asymmetry source is the gate bias circuit of the CG amplifier in the cascode structure. The simulated imaginary impedance at the gate of the CG amplifier is shown in Fig. 8(b) when a large series resistor, 16 kΩ, is used to make the RF open, which is a widely used bias circuit in previous works [2]–[7], and [9]. Given that large resistive gate biasing is used at the virtual ground node of the CG amplifier, the gate impedance starts to decrease due to parasitic gate capacitance in CG amplifier with the increase of the frequency [22]. This changes the imaginary part of the impedance very much and causes a large phase difference at Δf and the resultant large IMD3 asymmetry.

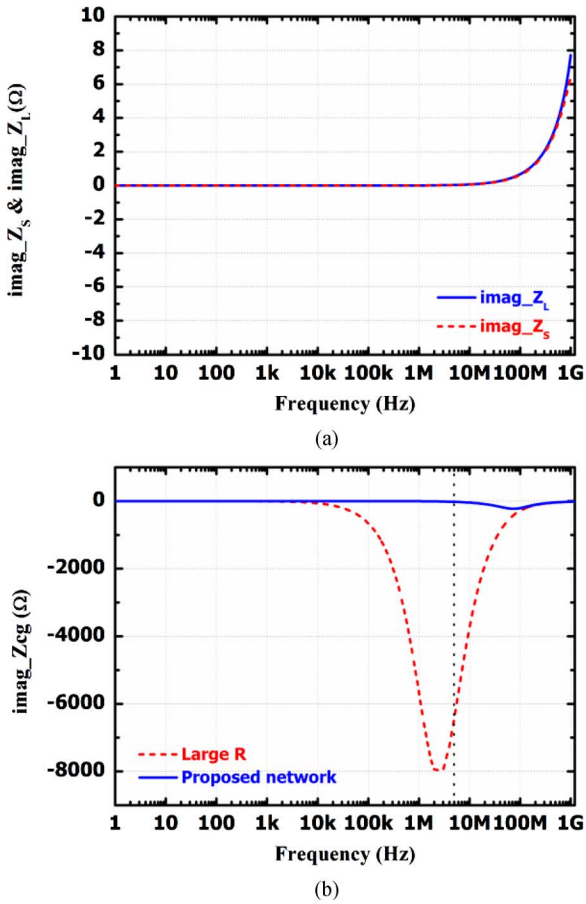


Fig. 8. Simulated imaginary impedance of designed PA (a) at load, source, and (b) the gate of CG amplifier with two different bias network conditions.

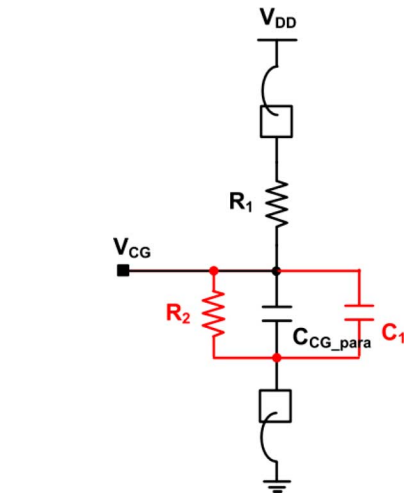


Fig. 9. Schematic of the proposed bias network at the gate of CG amplifier.

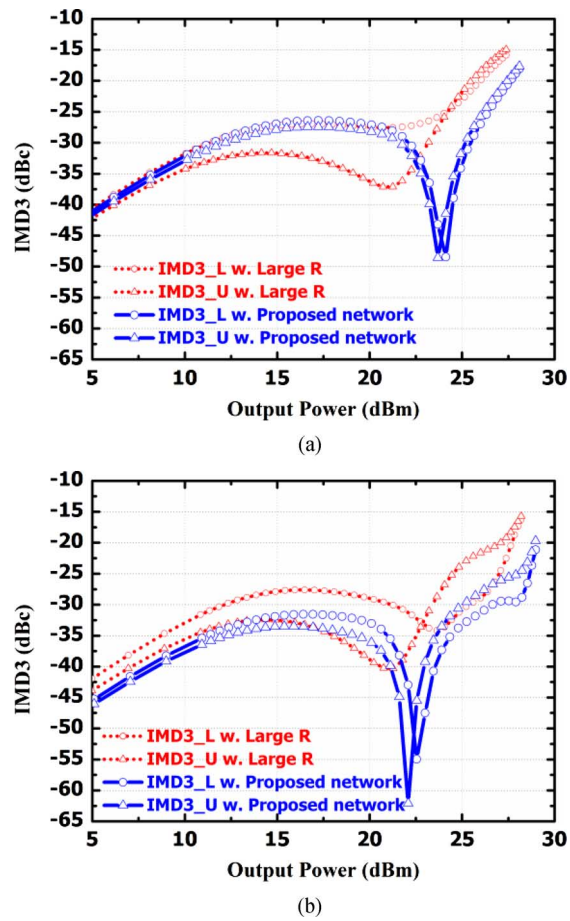


Fig. 10. Simulated IMD3 for two different bias networks at the gate of CG amplifier (a) without and (b) with reshaped envelope signal injection to the gated of CS amplifier.

C. Second-Order Nonlinear Components Control via a Bias Circuit

To remove the sideband asymmetry, the imaginary impedance is set to have a constant or low value at both the source and load over a wide frequency range. Thus, the impedance at a low frequency must be terminated in a short-circuit condition [21]–[28]. This consideration regarding the gate bias circuit of the CG amplifier is also necessary in a differential cascode structure with input and output BALUNs. The imaginary impedance of the proposed bias circuit to control the second-order nonlinear components in the gate of the CG amplifier and its schematics are shown in Figs. 8(b) and 9. Because this makes the imaginary impedance ($\mathrm{imag\_Z_{CG}} = -22.3\ \Omega$) at Δf that is much smaller than the previous RF open ($\mathrm{imag\_Z_{CG}} = -6.4\ \mathrm{k}\Omega$) case, the sideband asymmetry is reduced, as shown in Fig. 10. It also included the simulated results, without and with the reshaped envelope signal injection to the gate of CS amplifier. Since the gate bias of the CS amplifier is changed by Δf, the simulated results in Fig. 10(b) show that there are additional IMD3 asymmetries at high power region. Moreover, if we choose the impedance at the $2\mathrm{f}_0$ properly, the IMD3 magnitude is reduced near the maximum linear power as shown in Fig. 10. A bond-wire and capacitors, including the parasitic gate capacitor, $\mathrm{C_{CG\_para}}$, in the differential CG amplifier and the parallel capacitor are used in the bias circuit to optimize the impedance at $2\mathrm{f}_0$. The simulated IMD3s with various capacitances, C_1 in Fig. 9, ranging from 0 pF to 3 pF in the proposed gate bias circuit of CG amplifier are shown in Fig. 11. The bias circuit draws 2 mA from the power supply, which is quite small compared to that of the power stage.

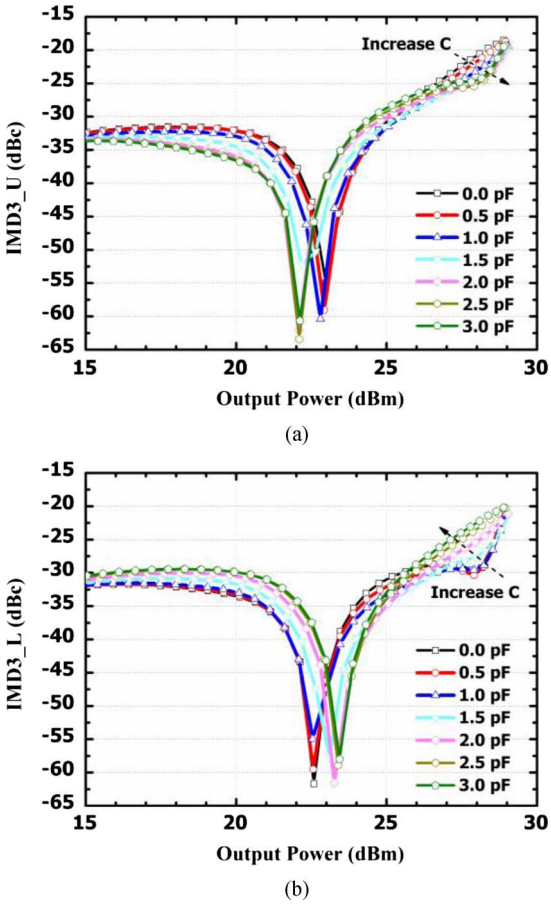


Fig. 11. Simulated IMD3 with various capacitances, C_1 in Fig. 9, ranging from 0 to 3 pF in the proposed gate bias network of the CG amplifier. (a) Upper IMD3. (b) Lower IMD3.

IV. Implementation and Measurement Results

A. Implementation

Fig. 12 shows a schematic of the designed single-stage differential cascode PA. It includes the two proposed gate bias circuits to improve the linearity. A differential cascode structure is used to moderate the voltage stress in each transistor which has a low breakdown voltage and to reduce the effects of the bonding wires at the source of the common source amplifier. A feedback network, with the series resistor ($R_F = 140\ \Omega$) and capacitor ($C_F = 1$ pF), is used between the drain of the CG amplifier and the gate of the CS amplifier to improve the stability and linearity of the PA [35]. The gate length of MP_1 is 0.18 μm and that of the thick oxide device, MP_2, is 0.4 μm. The total gate widths of MP_1 and MP_2 are 4096 μm and 5120 μm, respectively.

Due to the differential power stage, the virtual ground of the input BALUN is used to apply the bias [7] and [12] that is generated by the proposed Class-D bias circuit, for the reshaped envelope signal injection. The line width of the input BALUN is 5 μm and the spacing between each line is 2.5 μm, with the 3 μm thick copper metal. An unbalanced input of the input BALUN is used as the RF input and the input of the proposed Class-D bias circuit. The output matching network is completed by a TLT, including two matching capacitors on an integrated passive device (IPD) which contains the 10 um thick copper metal and highly

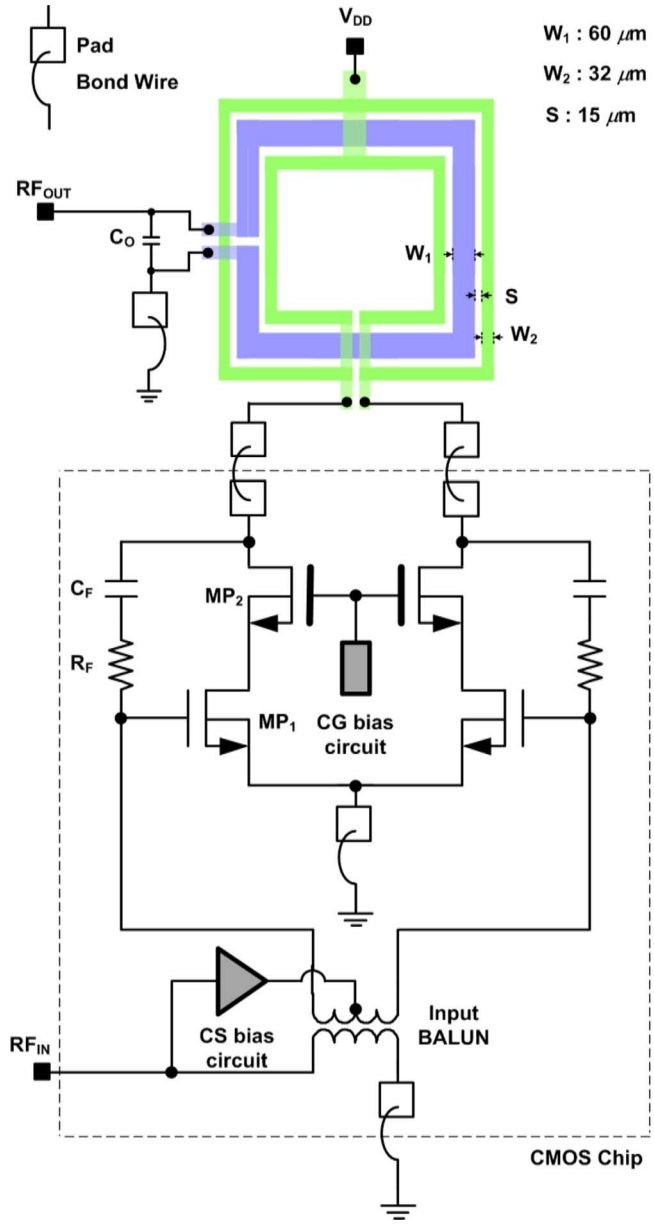


Fig. 12. Schematic of the designed CMOS PA with IPD TLT.

resistive substrate [5] and [6] to improve the efficiency. The primary line of the output TLT is also separated into two parts, each 32 μm, to reduce the insertion loss by increasing the coupling factor [36]. The secondary line width of the output TLT is 60 μm and the spacing between the lines is 15 μm. The insertion loss of the output matching network was found in a simulation to be only 0.74 dB ($MAG = -0.66$ dB) at 1.85 GHz, showing that it was less than 0.8 dB from 1.75 to 1.95 GHz.

Finding the optimum output impedance is the most important aspect when designing a PA. The output impedance determines the overall performance of a PA, including the power gain, output power, efficiency, and linearity. There is a tradeoff between efficiency and linearity, and these are two important parameters, especially in linear PAs. The optimum load was selected from the 1 dB compression and two-tone load pull simulations. The 1 dB compression load pull finds the optimum

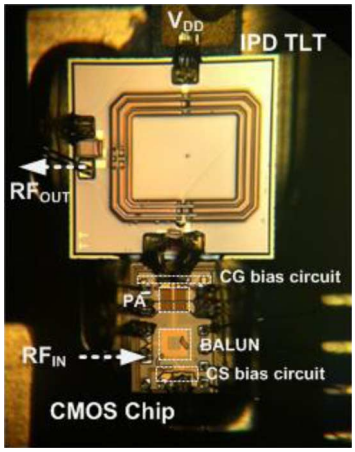


Fig. 13. Die photo of the designed CMOS PA ($475 \times 825\ \mu m^2$) with IPD TLT ($1300 \times 1300\ \mu m^2$).

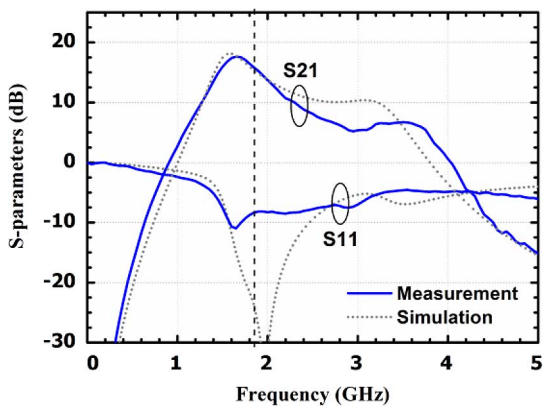


Fig. 14. Measured S-parameters versus frequency when P_{IN} is -20 dBm.

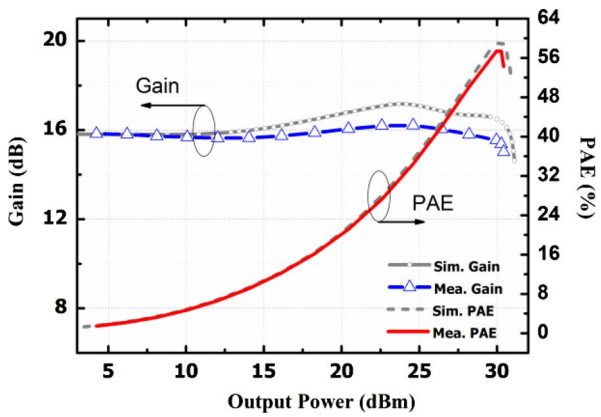
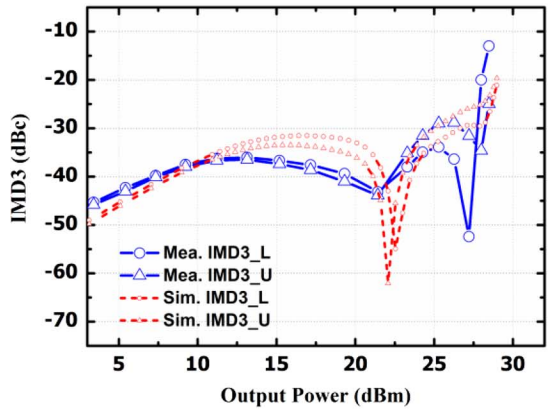
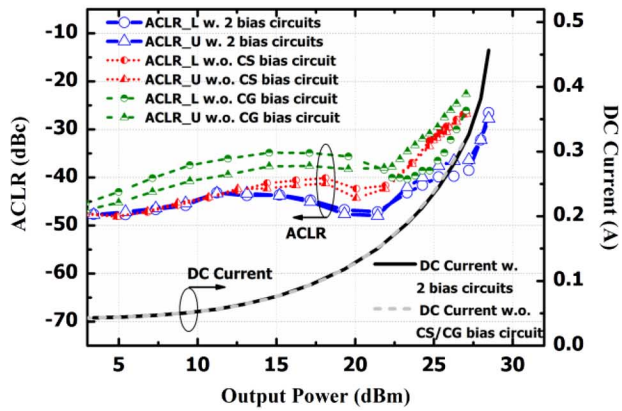


Fig. 15. Measured power gain and PAE versus output power under the CW test at 1.85 GHz.

impedance that provides the highest output power and highest efficiency with the minimum AM-AM distortion at various CW input powers. Because the gain is primarily changed using the gate bias, the load impedance is more important for the PA with the proposed bias circuit to have higher 1 dB compression output power and efficiency than with a fixed gate bias. The two-tone load pull with a tone spacing equal to channel offset in WCDMA applications, 5 MHz, obtains the optimum



(a)



(b)

Fig. 16. Linearity test of the designed PA at 1.85 GHz. (a) Measured and simulated IMD3. (b) Measured ACLR at 5 MHz offset using WCDMA signal.

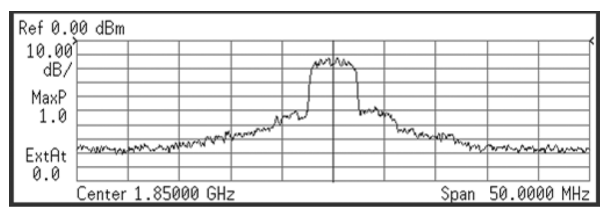


Fig. 17. Measured WCDMA output spectra at $P_{OUT} = 26.8$ dBm.

impedance that has the lowest third-order intermodulation distortion (IMD3) at a high-power region. Because the peak to average ratio (PAPR) of the WCDMA modulated signal, 3.5–4.5 dB, is not far from that of the two-tone modulated signal, 3 dB, the linear output power was estimated using the two-tone simulation. The linear output power was set at -25 dBc of the IMD3, which passes the WCDMA spectrum mask of -33 dBc ACLR at a 5 MHz offset.

B. Measurement Results

The two chips, the PA core including bias circuits using 0.18-μm CMOS technology and an output matching network using IPD, are presented in Fig. 13. The chips were mounted closely on an FR4 board and several bond wires are used for the test. The performance of the PA was assessed by driving the amplifier with an RF signal generated using an Agilent E4438C vector signal generator and ZVE-8G as a driver amplifier.

TABLE I
PERFORMANCE COMPARISON OF RECENTLY REPORTED WCDMA HANDSET PAS

Ref.	Technology	P_{OUT} (dBm)	PAE (%)	Gain (dB)	ACLR @P_{OUT}	V_{DD} (V)	Freq. (GHz)	Output matching networks	Characteristic
Jager 02 [37]	InGaP/GaAs HBT	27	38	22.6	-37 dBc	N/A	1.95	Off-chip	Broadband PA
Srirattana 03 [38]	GaAs FET	29.7	46	8.5	-38 dBc	N/A	1.95	Off-chip	3-stage Doherty PA
Zhang 09 [39]	InGaP/GaAs HBT	28	44.5	N/A	-38 dBc	3.4	1.95	Off-chip	Balanced PA
Wang 04 [8]	CMOS 0.5 μm	24	29	23.9	-35 dBc	3.3	1.75	Off-chip	Capacitive Comp.
Jeon 10 [9]	CMOS 0.18 μm	23.5	40	26	-33 dBc	3.4	1.95	On-chip L-C	Feedback bias
Pornpromlikit 10* [10]	SOI CMOS 0.13 μm	29.4 28.5	41.4 38.7	14.6	-33 dBc -38 dBc	6.5	1.9	Off-chip	Stacked FET
This works	CMOS 0.18 μm	27.8 26.8	45.8 43.3	15.8	-33 dBc -37 dBc	3.5	1.85	IPD TLT	CS & CG bias circuits

* These results are under 6.5 V supply, the expected maximum linear power near 22.5 dBm with 35% PAE from measurement in [10] under 3.5 V supply

The output power and spectral characteristics, IMD3 and the adjacent channel leakage ratio (ACLR), were measured using an HP437B power meter and an Agilent E4406A vector signal analyzer. The initial bias conditions of the power amplifier, when no input signal enters at the input, are a supply voltage of 3.5 V and 43 mA including bias circuits. All measurements of the power performance start from these quiescent current conditions.

Fig. 14 shows the simulated and measured S11 and S21 as a function of frequency. The measured S11 and S21 are -8.6 dB and 15.8 dB at 1.85 GHz. Fig. 15 shows the measured power gain and efficiency with respect to the output power at 1.85 GHz including the simulated results. There are some differences between the simulated gain and the measured gain, since the simulated one shows the gain expansion. The PAEs are found to be quite similar. The measured P_{sat} is 30.5 dBm. Fig. 16(a) shows the simulated and measured IMD3 as a function of the average output power. There are some differences between the simulated IMD3 and the measured IMD3, especially in high-power regimes, but the overall shapes are very similar. Fig. 16(b) shows the measured ACLR and DC current as a function of the average output power using an uplink WCDMA signal at 1.85 GHz with three different bias circuits; the first one uses the proposed bias circuits at CS and CG amplifiers, the second one uses the proposed bias circuit only at CS amplifier with a large resistor (16 kΩ) for the gate bias at the CG amplifier, the last one uses the proposed bias circuit only at a CG amplifier with fixed gate bias at CS amplifier, respectively. The output power securing the linearity margin, -37 dBc ACLR at a 5 MHz offset and -54 dBc ACLR at a 10 MHz offset, is 26.8 dBm with 43.3% PAE at 1.85 GHz. The maximum output power satisfying the WCDMA linearity specifications, -33 dBc ACLR at a 5 MHz offset and -44.7 dBc ACLR at a 10 MHz offset, is 27.8 dBm with 45.8% PAE at 1.85 GHz. The increase of the maximum linear output power and PAE are as much as 3.1 dB and 10.8% respectively, compared to without a CS bias circuit to inject reshaped envelope signal case. At the maximum linear output power, the total current of the CS bias circuit is less than 4 mA. The maximum ACLR difference is reduced from 10.4 dB to 2.7 dB depending on the gate bias circuit of the CG amplifier.

The measured output spectra at $P_{OUT} = 26.8$ dBm is shown in Fig. 17. Table I summarizes the measurement results and compares them with the previously reported results in WCDMA handset PAs. To the best of the author's knowledge, this work shows the highest efficiency reported yet for a WCDMA CMOS PA meets linearity requirements. It is comparable to GaAs-based PAs in terms of both linearity and efficiency.

V. CONCLUSION

We demonstrated linearization techniques using the proposed integrated gate bias circuits in a differential RF CMOS cascode PA. A Class-D bias circuit, which injects the reshaped envelope signal into the gate of the CS amplifier, compensates the gain degradation in the PA and thus reduces the additional distortion caused by the distorted injection signal. This bias circuit improves the maximum linear power by 3.1 dB, and PAE 10.8%. Control of the second-order nonlinearities at the gate of the CG amplifier also reduces the IMD3 asymmetry and the magnitude near the maximum linear power. This bias circuit reduces the ACLR asymmetry by 7.7 dB. Using an uplink WCDMA signal with a 3.5 V supply voltage, the PA shows an average output power as high as 27.8 dBm with a PAE of 45.8% while meeting the ACLR requirement. High linearity and efficiency are comparable to those noted in GaAs-based PAs. Thus, the proposed method of two gate bias circuits becomes an attractive solution in the design of a linear CMOS PA.

ACKNOWLEDGMENT

The authors would like to thank K. Y. Son and T. Joo, Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, for their helpful advices and discussions. The authors also acknowledge H. Hwang, G. Kim, M. Jeong and

H. Paek, Samsung-Electro-Mechanics, Suwon, Gyeonggi-Do, Korea, for their support.

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