A Digital CMOS Design Technique for SEU Hardening

Mark P. Baze, Steven P. Buchner, and Dale McMorrow

***Abstract*—A new cell design technique is described which may be used to create SEU hardened circuits. The technique uses actively biased, isolated well transistors to prevent transients in combinational logic from reaching the output node.**

I. Introduction

A LOGIC cell design technique has been developed which uses a new method of transistors placed within actively biased, isolated wells for SEU transient hardening. Active biasing of isolated wells is used to create low field transistors with reduced transient SEU response. These transistors are used within the logic cell to form transient hardened connections to the cell's output nodes. The impedence of these transistors is then set to block and dissipate transient pulses originating in any other transistors in such a way that the output node of the cell remains in the correct logic state. We call this technique "isolated well hardening."

Isolated well hardening may be applied to create a wide range of SEU hardened register and combinational logic functions. Because it prevents transients in combinational logic from reaching the cell output nodes, it is also applicable to dynamic logic.

II. Background

Traditional circuit design methods for dealing with SEU have focused on the memory and register elements of digital circuits because these elements are usually the largest contributors to single event error rates. Methods for mitigating SEU in these include circuit redundancy, resistive dissipation, capacitive dissipation, and high current recovery [1]–[7]. In nearly all of these cases, hardening is achieved by preventing the SEU transient pulses in memory and registers from becoming static bit errors. Only a few techniques have addressed this problem by actually attempting to prevent the collected charge from becoming a transient logic error [8].

As CMOS feature sizes continue to shrink, it is expected that the combined influences of reduced switching charge and higher clock rates will cause the single event error rates in combinational logic to become an issue that must be addressed directly to achieve adequate SEU hardness. In recent design work at Boeing using both a 0.4 and a 0.8 micron SOI process, the predicted logic induced error rates in a number of circuits were sufficient to require circuit level hardening. Of particular concern were logic cells on multiple rate, synchronous clock lines for which a single transient could result in multiple bit errors.

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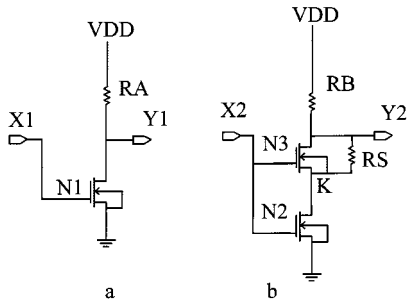

Fig. 1. (a) Simple soft and (b) hardened NMOS inverters.

III. Description

A. Simple NMOS Illustration

Fig. 1(a) and (b) are a pair of very simple schematics that illustrate the concept behind isolated well hardening. Fig. 1(a) is a simple inverter consisting of a single NMOS transistor, N1, and a "pull-up" resistor RA. Fig. 1(b) is a similar inverter that has been hardened by the addition of transistor N3 and shunt resistor RS. The critical features of this method are, 1) transistor N3 is in a well that is separate and isolated from the well of N2 and 2) the well of N3 is actively biased by the drain of N2 and resistor RS.

The inverter of Fig. 1(a) is in an SEU sensitive state when the input X1 is low and the output Y1 is high. In this state there is a strong field across the drain-well junction of N1. If a heavy ion hit produces sufficient charge near the drain-well junction of N1, that charge will be collected by the field, reduce the voltage on the drain node, and result in a transient error on Y1.

In the case of circuit b, a low state on X2 will result in a strong field across the drain-well junction of N2. Resistors RB and RS will pull both nodes Y2 and K high. N3 will also be in a high impedance state, but since the source, drain, and well of N3 are all at nearly the same potential there will be no strong fields at either the source-well or drain-well junctions of N3. Due to this absence of strong fields in N3, the currents resulting from ion hits to N3 will be too small to produce appreciable transient errors on Y2. If an ion hit occurs near the high field region in N2, there may be sufficient collected charge to drive node K to ground, but since N3 is in a high impedance state, the main current path to VDD will be through RS and RB. The magnitude of the voltage transient on Y2 will be

$$\mathrm{VDD} \times \mathrm{RB}/(\mathrm{RS} + \mathrm{RB}). \quad (1)$$

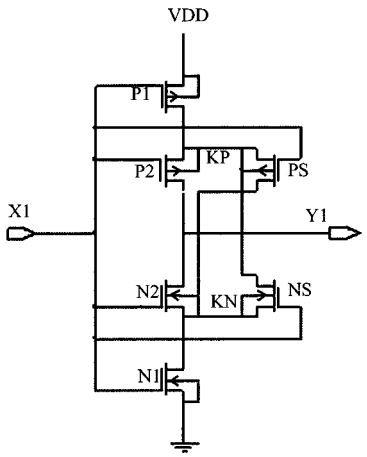

Fig. 2. SEU hardened inverter in an SOI process.

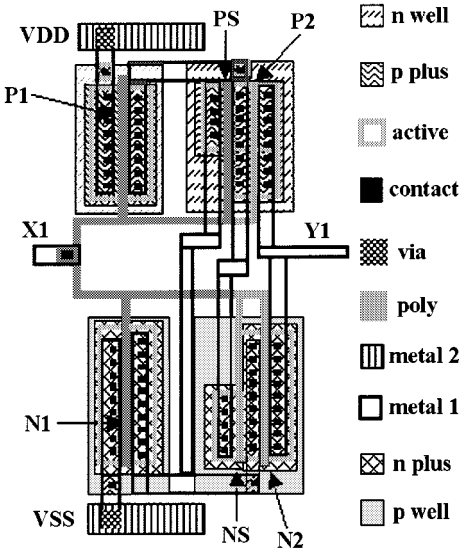

Fig. 3. Physical layout for the inverter in Fig. 2.

Since RS $\gg$ RB the transient on Y2 due to a hit to N2 will be $\ll 1/2$ VDD.

B. CMOS SOI Implementation

While Fig. 1 is useful for discussion, implementing this schematic in a CMOS technology would be impractical due to the large physical size of the resistors. A more practical implementation of this design technique is the schematic for a CMOS SOI version shown in Fig. 2. Well connections in this schematic may be considered equivalent to what are termed body ties or body contacts in some SOI technologies. In this figure, the shunt resistor RS has been replaced by transistor NS, and RB by the PMOS complement of transistors N1, N2, and NS. Low field conditions are maintained for transistors PS and NS by making the well and source connection of PS in common with the well and source connection of P2 and the well and source connection of NS in common with the well and source connection of N2. Transistors PS and NS are also sized smaller (approximately half as large) than P1 and N1 to provide the appropriate shunt current drive.

Since the configuration in Fig. 2 requires separate isolation and active bias of both p-wells and n-wells, it is best implemented in a process such as SOI which has the capability for building separate, dielectrically isolated well, or body, regions with individual well connections or body ties. A representative layout for this inverter in a trench sidewall SOI process is shown in Fig. 3.

C. Bulk CMOS Implementation

The circuit in Fig. 2 cannot be built in a standard junction isolated bulk or epi-CMOS process because there is only one "type" of well (either p or n) that can be isolated. The complementary type (n or p) is a global layer, either the epi- or substrate. However, a modified version of Fig. 2, which uses only one type of well, can be built. Fig. 4 is a schematic showing how this hardening method has been applied to a bulk CMOS n-well process. In this circuit there is only one shunt transistor, PS and transistor NS in Fig. 2 has been eliminated. Transistor N2 in Fig. 2 has been replaced by P4, which is placed in its own

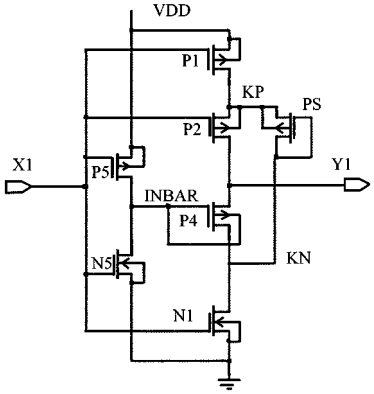

Fig. 4. SEU hardened inverter in a bulk n-well process.

isolated n-well. Transistors P5 and N5 have been added to provide proper bias to the gate and well of P4.

Fig. 5 is a representative layout for this circuit. An analogous circuit can also be built in a p-well bulk process by using the n and p type complements of the transistors in Fig. 4.

This bulk CMOS design does have two SEU vulnerable regions that are not present in the SOI design. Both of these regions are sensitive when X1 is high. In one case the n-well of transistor P4 is low and there is a high field across the well-substrate junction. An ion hit to this junction can result in charge collection at the source of P4 and a transient on Y1. In the second case, a hit to N5 will cause a positive transient on INBAR. In this condition the substrate-source junction of P4 becomes forward biased and a transient can again appear on Y1. The vulnerability of both these regions is described in the laser test results.

IV. Test Circuits

Four test circuits were fabricated to experimentally determine the validity of this hardening approach. Two were built in a 0.8 μm CMOS SOI process, one using the inverter shown in Figs. 2 and 3 and another using standard 2X drive inverters. Two more were also built in a 0.5 μm bulk CMOS process, one using

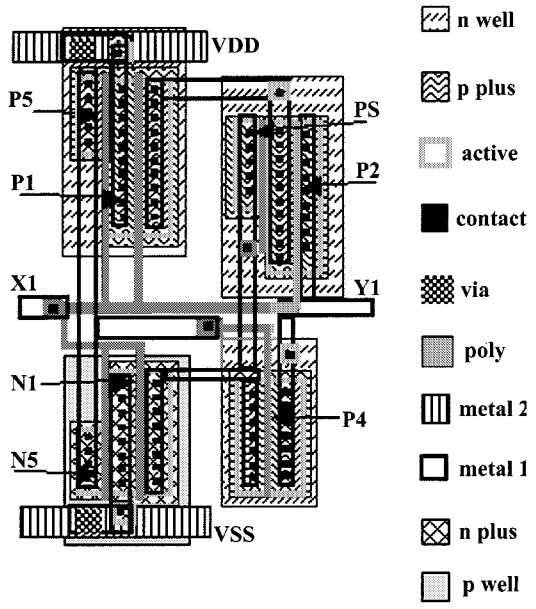

Fig. 5. Physical layout for the inverter in Fig. 4.

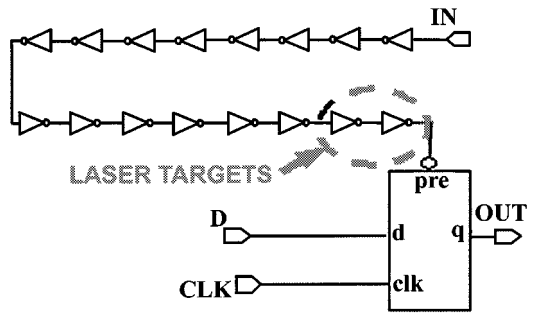

Fig. 6. Gate level schematic of the test circuits.

the inverter shown in Figs. 4 and 5 and one using standard bulk 2X drive inverters. The SOI process has an active layer depth of 0.25 μm for charge collection. The depletion depth of the bulk process as estimated by the manufacturer is approximately 1 μm and the collection depth due to funneling an additional 4 μm.

Fig. 6 is a gate level schematic common to all four test circuits. If IN is held "high," D "low," and CLK is cycled once "low–high–low," then OUT will be "low." This is the test bias condition. In this condition, a transient of sufficient width on the PRE input of the flip/flop will trigger the preset function and set OUT to "high."

The flip/flop serves as a threshold transient pulse detector because the pulse widths of single event transients are often too short to propagate to the output pads for measurement. The PRE input of this particular flip/flop is the most sensitive register input in our design library in that it responds to a shorter input pulse width ($\sim$300 ps) than any other in the library to switch the register's output.

The choice of 2X drive inverters for the soft circuits was made to facilitate laser testing. Most of the transistors in the hardened inverters were copied from 2X drive inverters. Using the same transistors in both structures serves to preserve the geometric relationships of charge collection regions and masking from overlying metal and poly-silicon layers. Having geometrically identical laser targets allows for comparison of relative upset vulnerabilities by direct comparison of the laser pulse energy.

TABLE I
SPICE MODELED RESULTS

	Qcrit (pC)	LET_{EST} (MeV-cm^2/mg)	
Bulk			
Flip/Flop	0.21	4	
Soft inverter	0.43	8	
Hard inverter	0.82	16	
SOI		normal	parallel to gate
Flip/Flop	0.19	74	7.2
Soft inverter	0.26	99	14
Hard inverter	immune	immune	immune

The transistors in the hardened inverters were sized as follows: 2X drive strength sizing was used for P1, P2, P4, N1, and N2, and 1X drive strength sizing was used for NS, PS, P5, and N5. Supply Vdd for both circuits was 5 V.

V. SPICE SIMULATION RESULTS

Prior to testing, SPICE simulations were performed to calculate critical charges (Qcrit's) for upset and estimate threshold LET's according to the relationship:

$$\text{LET}_{\text{EST}} = 96.9 \times \text{Qcrit}\,(\text{pC})/L_{\text{EST}}(\mu\text{m}) \qquad (2)$$

where L_{EST} is the estimated charge collection length and LET_{EST} is the estimated LET in MeV-cm^2/mg. The upset criterion for these simulations was generation of a logic "high" on the circuit output, OUT in Fig. 6.

In both the SOI and bulk type inverters, ion hits to transistors N1 and P1 were simulated by pulsing erroneous states on nodes KP and KN. None of these simulations produced an upset at any pulse duration. In fact the largest voltage change to the outputs of the inverters was only 0.9 V. Ion hits to transistors P5 and N5 in the bulk inverter were simulated by pulsing erroneous states on INBAR. Hits to P5 did not result in upsets. Simulated hits to N5 of 0.82 pC (350 ps pulse width) or greater resulted in a static upset on OUT. With a manufacturer's estimated collection depth of 5 μm this corresponds to an LET threshold of 16 MeV-cm^2/mg.

For purposes of comparison, SPICE upset simulations were also performed for ion hits on the 2X drive soft inverters and for the internal nodes of the flip/flops. Results of the SPICE simulations are given in Table I. SPICE derived LET estimates for the SOI process are given for both normal and parallel incident ions. The former, representing a 0.25 μm collection length, is the quantity most easily measured in heavy ion beam testing, while the later, with a collection length equal to the transistor width, is the predominant contributor to error rate in an isotropic flux environment.

One limitation of SPICE is that it does not adequately simulate the low field currents that may result from hits to P2, N2, PS, NS, or P4. These cases were not SPICE simulated but were explicitly included in the laser tests.

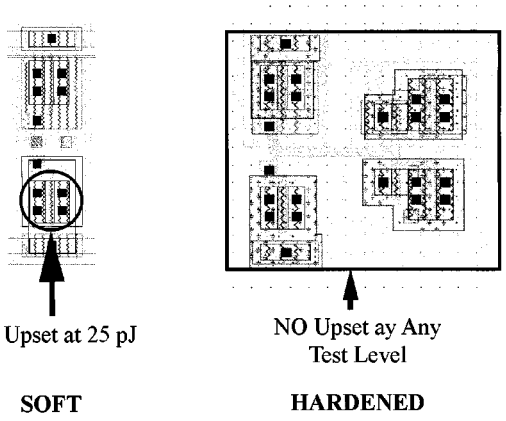

Fig. 7. "Mapped" laser results for SOI inverters. The hardened inverter did not upset.

Inverter Speed Penalty: Spice simulations also showed that the inverters in Figs. 2–5 have speed penalties when compared to standard soft 1X drive inverters. While the output current drives are comparable, the input capacitance of the hardened inverters is approximately 5 times that of soft 1X inverters. Modeling strings of inverters showed a 5X reduction in speed for the hardened string. This penalty in speed and is considered in the Discussion section below.

Bulk CMOS Logic "Low" Penalty: One additional penalty associated with the bulk hardened inverters is the presence of the PMOS pull-down transistor, P4, which makes the output low level 0.2 volts rather than 0 volts.

VI. Experimental Results

The test circuits described above were tested for relative upset vulnerability using the laser SEU simulation system at the Naval Research Laboratory. A full discussion of this system and the technique can be found in [9]–[11]. Laser testing was chosen over heavy ions because an experimental evaluation of this technique requires that test data be taken on the circuit upset responses from "hits" to specific geometric structures and because of the ease with which the laser can be utilized for this. While the absolute LET values derived from laser tests are not as accurate as those obtained in heavy ion testing [9], the relative values from the laser tests serve the goal of this work in demonstrating improvements in upset hardness.

Using a 605 nm wavelength the penetration depth of the beam was approximately 2.5 μm, sufficiently into the depletion regions of both the SOI and bulk structures. Within the sensitive regions shown in Figs. 7 and 8 the beam was focused on "open" regions outside of or between the reflecting metal and absorbing poly-silicon layers.

During laser testing the D inputs of the flip/flops were held "low," the inputs to the inverter strings were held "high," and the clock cycled "high" once and then held static "low." Under these conditions the outputs of the flip/flop's are normally a constant "low." If a transient error of sufficient width can be produced in the inverters, then the PRE input of the flip/flop will activate a static upset logic "high" on the flip/flop OUT that will hold until the next clock rising edge.

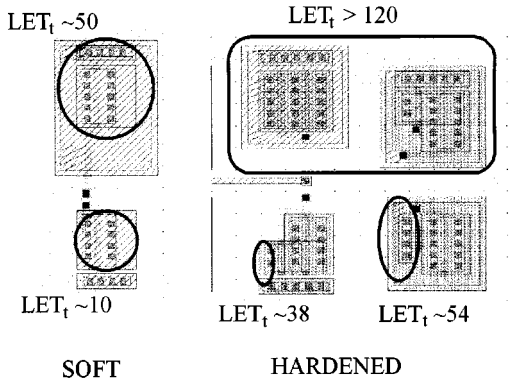

Fig. 8. "Mapped laser results for bulk inverters. LET's are in Mev-cm^2/mg.

TABLE II
Laser Simulation Test Results

	Energy (pJ)	Empirical LET$_t$ (MeV-cm^2/mg)
Bulk		
Flip/Flop	2	6
Soft inverter	4.3	13
Hard inverter	12.5	38
SOI		
Flip/Flop	8.2	25
Soft inverter	25	75
Hard inverter	immune	immune

Laser tests were performed on the hardened and unhardened inverters as well as the flip/flops in both the SOI and bulk processes. The upset thresholds obtained from these tests are listed in Table II. Laser energies were converted to LET using an empirically established equivalence of:

$$\text{LET(MeV-cm}^2\text{/mg)} = 3.05 \times \text{Laser Energy(pJ)} \qquad (3)$$

which has been shown to hold well for bulk and epi-processes [9].

Figs. 7 and 8 display the laser results relative to location for the inverters. Laser tests on the hardened SOI inverters yielded no upsets up to laser energies of 300 pJ. Fig. 8 shows that the upset threshold for the hardened bulk inverter occurs at transistor N5. In addition there is an upset region along the right edge of P4 that corresponds to the well-substrate vulnerability described earlier. Transistors P1, P2, P5, and PS showed no upsets up to the latchup threshold of this circuit, which is 120 MeV-cm^2/mg.

VII. Discussion

A. Penalties

Direct application of this technique to any given logic function carries certain penalties in speed, area, and power.

1) Speed: The speed penalty for 1X drive inverters was discussed above and was found to be a factor of 5 for a string of hardened as oppose to unhardened inverters. While there would be some variations depending on application, it is expected that this approximate reduction in speed would apply to other cells as well.

2) Area: The layouts shown in Figs. 7 and 8 are for the test inverters "as built." The height of these cells was set by the

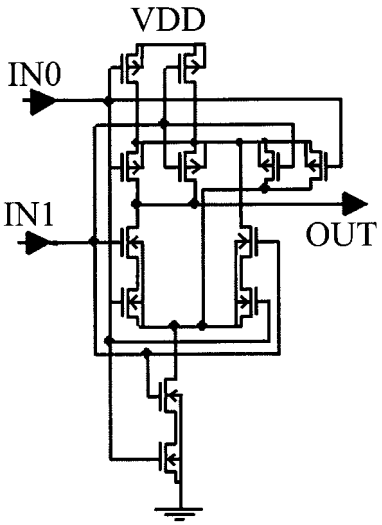

Fig. 9. SEU hardened NAND2.

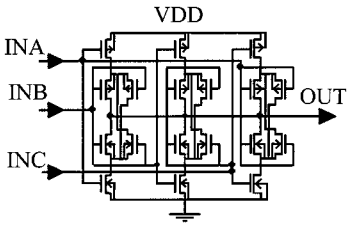

Fig. 10. SEU hardened VOTER.

power and ground rail spacing for the standard cell libraries. Thus, the soft and hardened cells have the same height. The width of the hardened inverters was approximately 3 times that of the soft inverters. These hardened inverters were not optimized for layout so some of the area penalty could be reduced, but an estimated penalty of 2.5 times the area is probably appropriate for most logic functions.

3) Power: On a cell by cell basis, the input capacitance of the isolated well hardened cells would result in approximately a 5X increase in power consumption. However on a chip level, power consumption is very dependent on the circuit design and application and is not always driven by the circuit's SEU vulnerable logic cells. For example if inherently SEU tolerant high power elements, such as I/O drivers, dominate a circuit's power consumption, then isolated well hardening of the logic would have less of an impact.

B. Applications

The only logic function that has been discussed up to this point is that of an inverter. It should be noted that any digital CMOS logic function could be constructed using this technique. Figs. 9–11 are examples of schematics for a nand, voter, and latch. This being the case, the only limits to the application of this technique are its practicality when compared to other techniques of hardening.

In cases where a single, simple logic function needs to be hardened, replacing that logic circuit with an "isolated well hardened" equivalent may be a reasonable option. However, for complex sequential logic IC's, the speed penalty of a cell

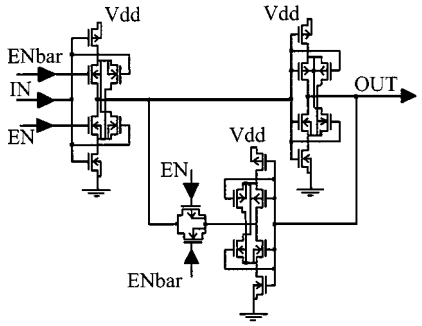

Fig. 11. SEU hardened LATCH.

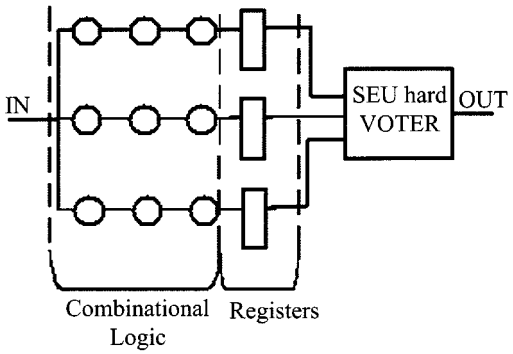

Fig. 12. Static bit and transient SEU hardened triplicate-and-vote strategy.

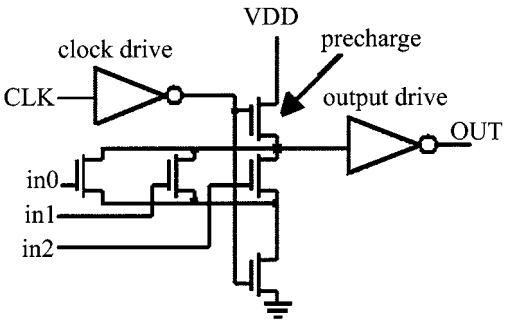

Fig. 13. SEU soft dynamic, clocked OR gate with "HOLD."

by cell replacement could be unacceptable. An alternative approach that has little impact on speed is to use a triplicate-and-vote strategy in which the logic and registers are standard unhardened cells and the voting circuit is the isolated well hardened voter from Fig. 10. Fig. 12 is a schematic of this approach. This circuit is only vulnerable to synchronous errors on more than one "branch" of the voted logic (i.e., single-hit multiple bit errors). It's penalties are 3X in power and area with only a modest (one voter delay) penalty in speed. Under similar voting schemes using unhardened voters the output would remain vulnerable to transients originating in the registers and the voter itself. In contrast, the output of the circuit in Fig. 12 is hardened to both static bit and transient upsets. This has important applications in clock and asynchronous control (i.e., resets) circuits where a single transient upset can propagate to cause a multitude of static bit errors.

Another area where this technique is applicable is in dynamic logic architectures. Since these do not use static storage elements, single event hardening techniques that focus on memory

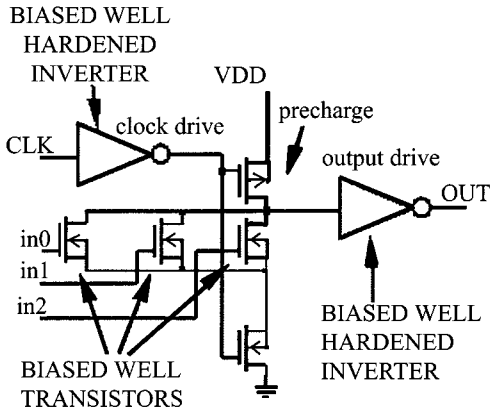

Fig. 14. SEU hard dynamic, clocked OR gate.

and registers are not applicable [12]. The isolated well technique provides a way to harden any of the combinational cells in a dynamic logic circuit. Fig. 13 shows an unhardened dynamic clocked or gate. Fig. 14 shows how this technique may be applied to build a hardened dynamic clocked or gate.

VIII. Conclusion

A CMOS logic design technique, using actively biased, isolated wells for single event upset hardening, has been developed and experimentally demonstrated. This technique develops transient upset immunity in an SOI process and a roughly 3X improvement in bulk CMOS logic. Since this technique hardens for both static bit and transient errors this technique has definite applications for clocks, asynchronous control logic and dynamic logic. Since the technique is scalable it should also be applicable to future increasingly vulnerable submicron SOI processes.

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