Submicron Ambipolar Nanocrystalline Silicon Thin-Film Transistors and Inverters

Anand Subramaniam, *Student Member, IEEE*, Kurtis D. Cantley, *Member, IEEE*, Harvey J. Stiegler, *Member, IEEE*, Richard A. Chapman, *Fellow, IEEE*, and Eric M. Vogel, *Senior Member, IEEE*

***Abstract*—Nanocrystalline silicon (nc-Si) thin-film transistors (TFTs) fabricated at a maximum processing temperature of 250 °C operate with high field-effect mobility compared with amorphous-silicon TFTs. By reducing the oxygen content in the channel layer, ambipolar behavior can be obtained. Two levels of electron-beam lithography are employed to fabricate nc-Si TFTs with nanoscale dimensions that operate without significant short--channel effects for gate lengths down to 200 nm. The TFTs have current–voltage (I–V) characteristics with on–off ratio $> 10^5$ at ± 1 V drain voltage and low threshold voltage shift. Simulation Program with Integrated Circuit Emphasis (SPICE) software is used to model the TFTs, and it is validated by performing the fit to devices of different dimensions. An inverter constituent of nc-Si TFTs offers high voltage gain (10–12) and frequency response better than 2 MHz. The crowbar current associated with the inverter can be minimized by using an optimized geometry ratio based on the leakage currents of the TFTs. An amplifier circuit is also demonstrated, offering an ac gain in the frequency range of 100 Hz–10 kHz. SPICE simulations of the inverter and amplifier show close agreement with measured data. The fabricated devices are well suited for use in high-density architectures.**

***Index Terms*—Amplifier, frequency response, inverter, nanocrystalline silicon (nc-Si), nanowires, SPICE, thin-film transistor (TFT).**

I. Introduction

NONCRYSTALLINE silicon [amorphous silicon (a-Si) or nanocrystalline silicon (nc-Si)] has been the object of much interest recently for use in applications that require large-area deposition, low-temperature processing, and the use of glass or plastic substrates. Some of these applications include neuromorphic architectures [1] and as the switching element in flat-panel displays [2]–[4]. Noncrystalline silicon has several advantages compared to other candidates such as amorphous oxides. The processing technology for noncrystalline Si thin-film transistors (TFTs) is compatible with regular CMOS processing. This, in turn, enables 3-D integration of such TFTs with CMOS structures and hybrid systems where the neuromorphic circuitry is entirely contained in the interconnect levels with a CMOS core that performs fast digital computation [5], [6]. Since most of the proposed applications do not require high-speed operation, it is possible to use low supply voltages to drive circuits with noncrystalline silicon components, thus ensuring low power consumption.

Nanocrystalline silicon consists of silicon embedded in an amorphous matrix [7]. Transistors made with nc-Si can exhibit ambipolar operation, which provides for easy implementation of complementary circuits such as inverters. This is in contrast to amorphous-oxide TFTs, which operate only in n-channel mode and therefore require other devices to be integrated to achieve complementary circuits [8]–[10].

The major drawbacks of noncrystalline silicon include low carrier mobility [11] and threshold voltage V_T shift under bias stress [12], [13]. Employing nc-Si instead of a-Si as the channel material increases the field-effect mobility by more than an order of magnitude. The bias-stress-induced V_T shift can be also reduced by switching to nc-Si and also by lowering the impurity concentration in the channel layer.

This paper offers several important advancements over previously published ambipolar nc-Si TFTs [14], [15]. The first is the fabrication of nanoscale TFTs with no significant short-channel effects. Submicron channel length and width of individual transistors are required for use in high-density architectures such as neuromorphic systems [16]. Second, the I–V characteristics have been modeled with Simulation Program with Integrated Circuit Emphasis (SPICE) and used to accurately predict the behavior of nc-Si TFT-based inverters. Third, the use of a source/drain metal other than Cr in an ambipolar TFT is demonstrated, proving that the metal work function is the crucial factor in achieving ambipolar operation. Last, the TFTs are shown to be capable of operation at moderate frequencies (beyond 2 MHz) and are suitable for their intended applications.

In this paper, we describe the fabrication and characterization of nc-Si TFTs with ambipolar conduction. Section II describes the fabrication steps in detail. Section III examines the I–V characteristics of the TFTs, variation of mobility values with gate voltage, and scaling of on-current with device dimensions. This is followed by a description of the SPICE models used to fit the data in Section IV. The development of close-fitting

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A. Subramaniam, K. D. Cantley, and R. A. Chapman are with the Department of Electrical Engineering, The University of Texas at Dallas, Richardson, TX 75080 USA (e-mails: asubram3@utdallas.edu).

H. J. Stiegler is with the Department of Materials Science and Engineering, The University of Texas at Dallas, Richardson, TX 75080 USA.

E. M. Vogel is with the School of Materials Science and Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA, and also with the Department of Materials Science and Engineering, The University of Texas at Dallas, Richardson, TX 75080 USA (e-mails: eric.vogel@mse.gatech.edu).

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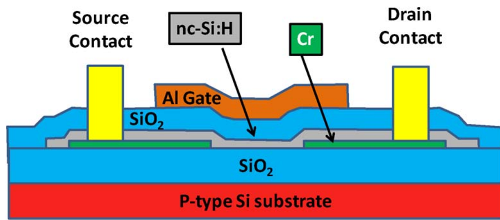

Fig. 1. Schematic cross section of a staggered top-gated nc-Si TFT.

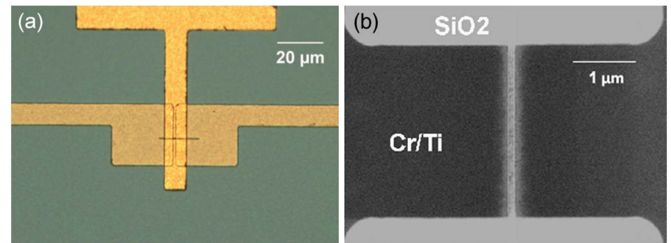

Fig. 2. (a) Optical microscope image showing a single 50-nm-wide nc-Si nanowire acting as the TFT channel. (b) SEM image showing a 200-nm channel in a nc-Si TFT. The dark area in the image is the source/drain metal, and the light area in the middle of the metal defines the channel.

SPICE models allows the prediction of how small circuits with nc-Si TFTs operate. The next section deals with inverter characteristics and their frequency response. Finally, an amplifier is presented and its operation is analyzed in detail.

II. Nanocrystalline Silicon TFT Fabrication

Hydrogenated nc-Si TFTs with staggered top-gated structure were fabricated with low-temperature processing (maximum temperature used was 250 °C). A p-type Si wafer (with doping 10^{17} cm^{-3}) was used as the substrate, on which 300-nm SiO_2 was grown with dry thermal oxidation. First, 80-nm Cr or Ti source/drain metal was deposited and patterned. Cr reacts with nc-Si forming chromium silicide contacts that are highly conductive and thus reduce electron and hole injection barriers [14]. Next, an 80-nm-thick nc-Si channel layer was deposited using plasma-enhanced chemical vapor deposition (PECVD) at 13.56 MHz, 125-W RF power, 0.9 torr, and 250 °C deposition temperature. Using a 1:100 mixture of SiH_4 and H_2 results in a nc-Si layer, as opposed to a 1:100 SiH_4 and He mixture, which provides a-Si. A turbo pump was fitted to PECVD to reduce the background vacuum pressure to 6×10^{-6} torr. This, in turn, results in a factor of 100 reduction in oxygen impurity content in the nc-Si layer, as shown by secondary ion mass spectroscopy analysis [17]. After channel patterning, a SiO_2 dielectric layer of 200-nm thickness was deposited also using PECVD at 250 °C. Vias were etched through the oxide, and contacts (100-nm Au) were deposited. The Al gate metal was then deposited and patterned by liftoff. The overlap between the gate and the source/drain electrodes was 5 μm each. Finally, the samples were annealed in forming gas at 250 °C for 2 h. Fig. 1 displays a cross section of the fabricated device.

Devices with submicron dimensions were fabricated by patterning the source/drain metal and nc-Si channel with electron-beam lithography (EBL). A dual-layer resist was used for EBL. The first layer is 60-nm polymethyl methacrylate, a positive-tone resist that is spun and baked at 180 °C for 1 min. The second layer consists of 35-nm 3% diluted Dow Corning XR-1541/hydrogen silsesquioxane (HSQ), a negative-tone resist that is spun and baked at 180 °C for 2 min. After exposure, development of the HSQ layer occurs in 8.5% tetramethyl ammonium hydroxide at room temperature for 1 min. Short-channel TFTs were fabricated by patterning the e-beam resist and then transferring the pattern to the source/drain metal layer by etching. Arrays of nc-Si nanowires with width of 50 nm each were used as the channel in nanoscale TFTs. The effective width is computed by multiplying the individual nanowire width by the number of nanowires. This arrangement resulted in less current crowding and lower subthreshold swings at low drain voltages than when using wider filled patterns [18]. Fig. 2 shows an optical microscope plan-view image of a patterned nc-Si nanowire and a scanning electron microscope (SEM) image of a submicron-length channel.

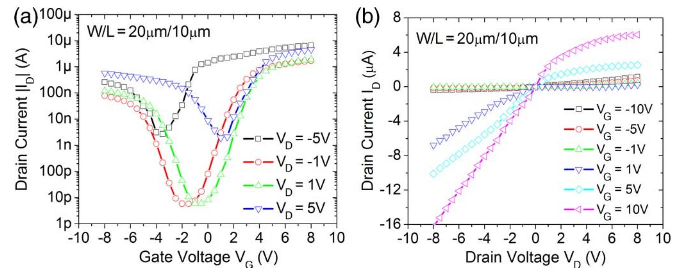

Fig. 3. (a) Transfer characteristics (in log scale) of a 20 μm $\times$ 10 μm ambipolar nc-Si TFT with Cr source/drain. (b) Output characteristics of the same device.

III. Electrical Characteristics

The electrical characteristics of the TFTs were measured using a Keithley 4200 characterization system and a Cascade Microtech probe station. The I–V characteristics when a 20 μm $\times$ 10 μm TFT is shown in Fig. 3. The transfer characteristics of a nanoscale (500 nm $\times$ 200 nm) TFT are shown in Fig. 4(a). The output characteristics of the same device are shown in Fig. 9(b). The individual nanowire width was 50 nm, and an array of ten nanowires was used, consequently making the effective width 500 nm. Both devices operate in the electron and hole regimes, i.e., display ambipolar operation. The direction of current flow solely depends on the drain voltage. Electrons constitute the charge flow when the gate voltage is positive, and holes when the gate voltage is negatively biased.

Very little hysteresis was observed in the I–V measurements, indicating the near absence of trap states in the channel layer. The use of Cr as a source/drain metal allows the formation of ohmic contacts with little or no barrier for the injection of electrons or holes. The reduction of oxygen in the channel layer is crucial in achieving ambipolar operation since oxygen acts as an unintentional n-type dopant [14]. The on/off ratio of the TFTs when operated at a drain voltage of $|1\text{ V}|$ is $> 10^5$, which is acceptable for most logic applications. As the drain voltage magnitude is increased, the on/off ratio reduces. This

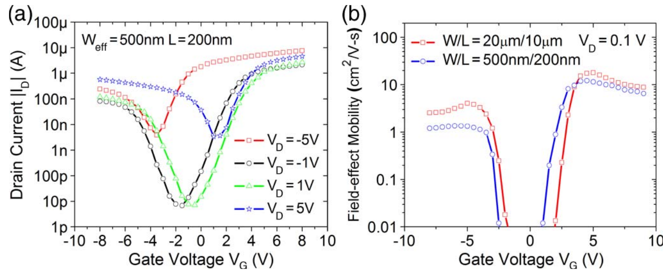

Fig. 4. (a) Transfer characteristics (in log scale) of a 500 nm × 200 nm ambipolar nc-Si TFT with Cr source/drain. Ten nanowires of 50-nm width each were used so that the effective width was 500 nm. (b) Comparison of the field-effect mobility values calculated at low drain voltage for nc-Si TFTs of different dimensions.

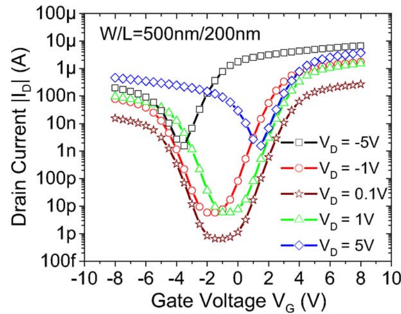

Fig. 5. Transfer characteristics (in log scale) of a 500 nm × 200 nm ambipolar nc-Si TFT with Ti source/drain. Ten nanowires of 50-nm width each were used so that the effective width was 500 nm.

arises because both hole and electron conduction take place for a larger range of gate voltages.

A comparison of the extracted field-effect mobility values of both devices is shown in Fig. 4(b). The mobility values were extracted at low drain voltage (100 mV). These values are among the highest observed in nc-Si TFTs [14], [15]. Using a top-gated structure aids in maximizing the mobility because carrier conduction takes place at the top interface of the channel where the crystalline volume fraction is generally the highest. In the n-channel regime, the 20 μm × 10 μm TFT has a threshold voltage V_T of 3 V and a subthreshold swing of 0.6 V/dec, whereas the corresponding values in the p-channel regime are −4 V and 0.65 V/dec. In the case of the nanoscale device, the n- and p-channel threshold voltages are 2.4 and −3.3 V, respectively. Furthermore, the on-current of the TFTs, measured at $V_G = V_D = 5$ V, linearly scales with both channel length and width down to 200 nm [17].

Ambipolar behavior was also observed in nc-Si TFTs with Ti source/drains (Fig. 5). These devices exhibited similar mobility values to the ones with Cr source/drains. All previously fabricated ambipolar TFTs with nc-Si channel layers used Cr as the source/drain metal [14], [15]. This result proves that different source/drain metals can be used for TFTs with ambipolar operation, provided that the contacts are ohmic (the work function of Ti is 4.33 eV compared with 4.5 eV for Cr).

The shift in threshold voltage upon the application of different voltage stresses was examined. I_D–V_G measurements were performed before and after the application of gate and drain bias stresses for set periods of time. Fig. 6 shows the results on a semilog scale. The magnitude of threshold voltage monotonically increased with stress time. The V_T shifts observed for electrons and holes were similar. In general, compared with previous results, the V_T shift is low for nc-Si TFTs [19], [20]. Small increases in the channel material deposition temperature are likely to decrease this degradation significantly.

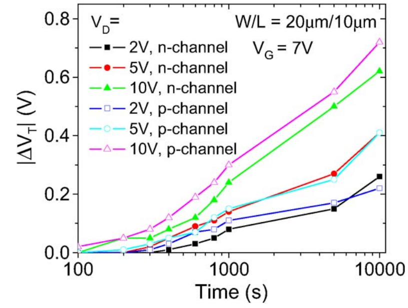

Fig. 6. Variation of the shift in threshold voltage with stress time for different applied bias values. The filled and open symbols indicate n- and p-channel measurements, respectively.

The observed V_T shift did not recover following a rest period of several hours or under the application of negative gate bias, suggesting that the shift is irreversible. The V_T shift commonly occurs through two mechanisms, namely, charge trapping in the gate dielectric and defect creation in the channel layer. Of these mechanisms, charge trapping in the gate dielectric is reversible [12]. Thus, under the applied bias conditions, defect state creation in the channel layer seems to be the dominant degradation mechanism.

I–V characteristics were also measured by grounding the top-gate bias and applying a bias to the bottom Si substrate. This arrangement causes the 300-nm SiO_2 grown on the substrate to act as gate dielectric. The same device in Fig. 3(a) was used. The results are shown in Fig. 7. Notice that, while the device still exhibits ambipolar operation, the threshold voltage is higher for both electrons and holes. The subthreshold swing is mostly unchanged. This result is linked to the way the crystalline volume fraction varies at deposition. The first few nanometers are mostly amorphous, followed by increasing crystalline volume fraction that stabilizes after approximately 40 nm. When the device is operated by using the substrate as gate, most of conduction occurs close to the bottom interface of the channel. This, in turn, leads to the degraded I–V characteristics. The drive current measured at $V_G = V_D = 5$ V decreases by 73% for the bottom-gate case compared with the top-gate case.

In addition, I–V characteristics were measured by applying different voltage biases at the substrate (instead of grounding it) and sweeping the top-gate bias. Fig. 8 demonstrates how the I–V characteristics shift upon varying the substrate bias. The shift in threshold voltage from when the substrate is grounded (initial case) for different voltages is given in Table I. All measurements were performed on a 20 μm × 10 μm device with drain voltage fixed at 0.1 V. The threshold voltages shift in the negative direction when positive substrate biases are applied to the transistor and vice versa. This shift is in accordance with [21] and [22], which establish the nonlinear relation between the back-gate bias and V_T due to charge coupling between the front and back gates through the active region of the TFT.

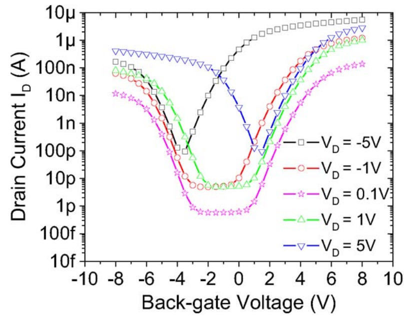

Fig. 7. I–V transfer characteristics of a 20 μm × 10 μm ambipolar nc-Si TFT when operated in the bottom-gate configuration (grounding the top-gate bias and sweeping the substrate voltage).

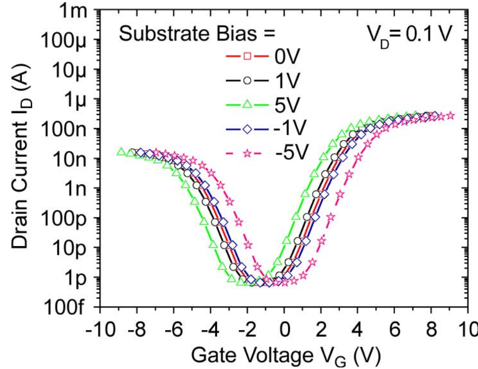

Fig. 8. I_D–V_G characteristics of a 20 μm × 10 μm ambipolar nc-Si TFT upon applying different substrate biases while sweeping the top-gate bias.

TABLE I
VARIATION IN THRESHOLD VOLTAGE WITH SUBSTRATE BIAS

Substrate Bias (V)	Shift in V_{Tn} (V)	Shift in V_{Tp} (V)
1	−0.25	−0.25
5	−0.85	−0.8
10	−2.35	−2.3
−1	0.2	0.25
−5	1.05	1.1
−10	2.25	2.25

IV. SPICE MODELING

It is important to predict how small-scale circuits employing nc-Si TFTs similar to the fabricated ones would behave. The AIM-SPICE MOS15 a-Si:H TFT model was used to fit the measured ambipolar I–V characteristics [16], [23]. The most significant model parameters were optimized using an algorithm that minimizes the least square error of the fit. A parallel combination of an n-channel TFT and a p-channel TFT was used to model a single ambipolar device. The minimum density of deep states was kept equal in both models because both contribute toward modeling a single TFT. The model was validated by performing the fit for different device geometries. The important parameters for the model are given in Table II. Note that the threshold voltage parameter, i.e., VTO, does not correspond to the actual threshold voltage of the modeled device, but rather, it is used to calculate the charge sheet density. Fig. 9(a) shows the transfer characteristics and corresponding SPICE model fit for a nanoscale nc-Si TFT. The output characteristics and model fit for the same device are shown in Fig. 9(b).

TABLE II
SPICE MODEL PARAMETERS FOR nc-Si TFTs

Parameter	Description	n-channel Model	p-channel Model
ALPHASAT	Saturation Modulation Parameter	1.6	1.5
DELTA	Transition Width Parameter	5	5
GAMMA	Power Law Mobility Parameter	0.07	0.05
GMIN	Minimum Density of Deep States	8×10^{21} /m^{3}eV	8×10^{21} /m^{3}eV
LAMBDA	Output Conductance Parameter	0.03	0.0001
M	Knee Shape Parameter	0.50	0.30
MUBAND	Conduction Band Mobility	20 cm^2/V·s	5 cm^2/V·s
VFB	Flatband Voltage	0.5 V	2.5 V
VTO	Zero Bias Threshold Voltage	−2 V	1.5 V

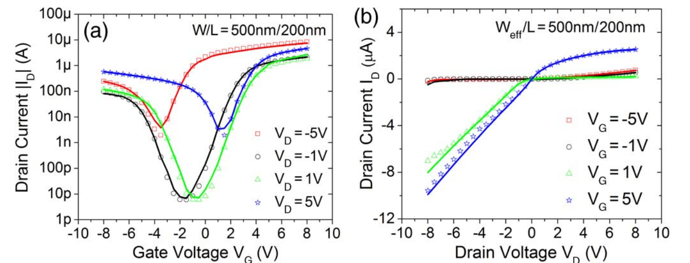

Fig. 9. (a) Transfer characteristics (in log scale) and corresponding SPICE model fit for a nanoscale ambipolar nc-Si TFT. The symbols represent data, and the lines represent the model. (b) Output characteristics and corresponding SPICE model fit for the same nc-Si device.

V. INVERTER CIRCUIT

As the first step toward implementing nc-Si TFT-based circuitry, an inverter circuit was fabricated using two of the nanoscale nc-Si TFTs and tested by sweeping the input voltage at different supply voltages. The pull-down TFT had dimensions $W/L = 100$ nm/200 nm, whereas the pull-up TFT had a width and length of 500 and 200 nm, respectively. The W/L ratio of the pull-up transistor is five times that of the pull-down device (β ratio $= 5$) to compensate for the lower hole mobility of the TFTs. The voltage transfer characteristics of the inverter for different supply voltages are shown in Fig. 10(a). A clear and abrupt transition from ON to OFF states was observed as the input voltage was swept. The slightly different threshold voltages of electron and hole conduction in the ambipolar TFT lead to asymmetry in the inverter voltage transfer curve. The slight increase in the output voltage at high input voltage ($V_{\rm in} > 5$ V) is due to the high off-current of the TFTs at high drain voltages. The inverter does not provide rail-to-rail swing due to current leakage, but it is comparable to other noncrystalline Si inverters. The experimentally extracted voltage gain ($V_{\rm gain} = \delta V_{\rm out}/\delta V_{\rm in}$) when operating at 6 V is 12, which is among the highest reported values using nc-Si TFTs [15], [24]. The operating voltage can be also lower than in some of the alternative inverters that employ low-temperature fabrication [8]. The output matched the corresponding SPICE simulation results closely [see Fig. 10(a)].

The "crowbar" current associated with a nc-Si inverter is crucial when calculating its switching power consumption.

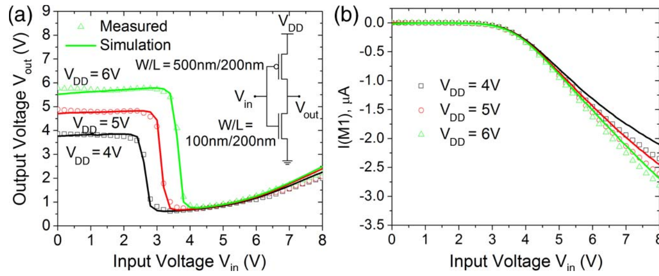

Fig. 10. (a) Voltage transfer characteristics of an inverter formed using two ambipolar nc-Si TFTs measured at different operating voltages, and corresponding SPICE simulations. The inset displays the inverter configuration. (b) Current flowing through the pull-up TFT as a function of the inverter input voltage and the simulation results for the same. The symbols represent data, and the lines represent the simulations in both plots.

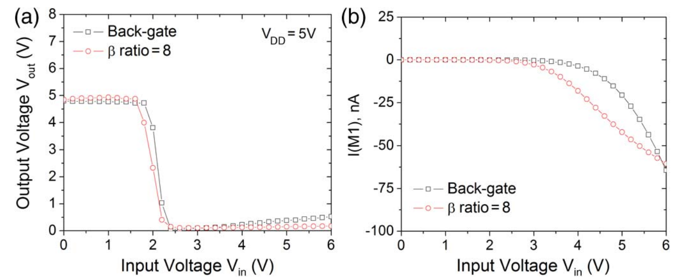

Fig. 11. (a) Comparison of the voltage transfer characteristics of a nc-Si TFT-based inverter when TFTs are operated in the back-gate configuration and when the β ratio is 8. $V_{DD} = 5$ V in both cases. (b) Comparison of the inverter currents in both cases.

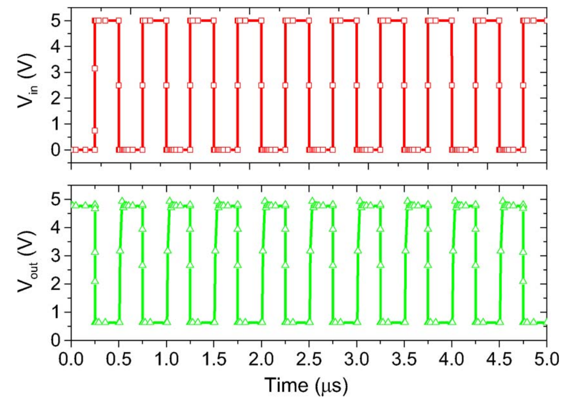

Fig. 12. Input pulse and output voltage of a nc-Si TFT-based inverter when the input frequency is 2 MHz.

Crowbar current refers to the current that flows directly from power supply to ground during switching events. The current flowing through the pull-up TFT is shown in Fig. 10(b). The current is a few microamperes at high V_{in}, and it does not significantly increase with V_{DD}. The simulated inverter current also matched the measurements. When switching at a rate of 100 Hz, the inverter's crowbar energy dissipation is approximately 5 pJ per switch. SPICE simulations were performed on the inverter circuit at the same bias conditions with capacitive load equivalent to another inverter at the output. From these simulations, the dynamic switching energy was calculated to be 20 pJ per switch. Therefore, the crowbar power dissipation is higher than ideally desired.

The ambipolar operation of the TFTs is the reason for the increase in crowbar current at high input voltages (and the consequent high crowbar power dissipation). Notice in Fig. 3 that, even at low drain voltages, there is only a narrow range of gate voltage in which the drain current is low. This leakage current can be reduced in two ways, i.e., by adjusting the geometry ratio of the inverter to balance the electron and hole conduction in both TFTs or by operating the TFTs in the back-gate configuration. Operating an inverter with TFTs in the back-gate configuration allows the larger off-current region (see Fig. 7) to be utilized, thereby reducing the inverter current. A β ratio of 8 was determined to be the best case to minimize inverter current and to achieve the best voltage output range possible (closest to rail-to-rail swing). Operating the TFTs in the back-gate configuration reduced the current by a factor of 23, whereas changing the β ratio to 8 reduced the current by a factor of 25. The voltage transfer curve and crowbar current for both cases are shown in Fig. 11. Either configuration promises considerable power savings.

In addition to the switching power dissipation, the high off-current of the TFTs at large drain voltages translates to nonzero power dissipation of the inverter while at rest. This can be reduced through the use of different source/drain contact metals or shifting the I_D–V_G curve by either using a gate metal with a different work function or applying a substrate voltage bias.

For the use in circuit applications, it is vital to know the dynamic characteristics of the inverter. The inverter frequency response was measured by feeding square pulses with 50% duty cycle as input to the inverter. The equipment used for these measurements includes an Agilent pulse generator and a Tektronix oscilloscope. The rise and fall times of the pulses were fixed at a very low value of 10 ns. The frequency of the pulses was varied from 100 Hz to 10 MHz. The inverter responded closely to the input until approximately 2 MHz, above which it exhibited an appreciable lag. This corresponds to a time delay of 500 ns, which is comparable with other inverters utilizing a low-temperature fabrication process [8], [25], [26]. However, the a-Si-based inverters offering similar delays operate at much higher voltages. The gate-to-source overlap capacitance of 0.86 nF/m is probably responsible for limiting the maximum operating frequency. SPICE simulations support the observed inverter frequency range. Operation in the current range of frequencies is sufficient for most applications of noncrystalline silicon devices, including neuromorphic [27] and flat-panel displays. Fig. 12 shows an input pulse and the corresponding output at 2-MHz operating frequency.

A nc-Si TFT-based inverter can be also used as the basis for a voltage amplifier. Fig. 13 shows the circuit diagram of such an amplifier where the input is a small-amplitude ac signal v_{in} superimposed on a dc voltage V_{IN}, which is the inverter turnover voltage. This ensures that the inverter operates with the highest static gain. In the case of our inverter, $V_{\mathrm{IN}} = 3.37$ V. The inverter was biased with a supply voltage of 5 V. The same TFT dimensions, as shown in Fig. 10(a), were used for the amplifier. Unlike the fabricated inverter, the amplifier was

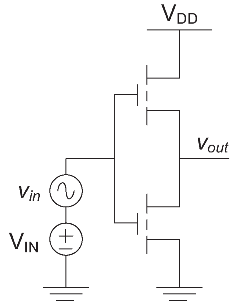

Fig. 13. Circuit diagram of an ambipolar nc-Si TFT-based amplifier.

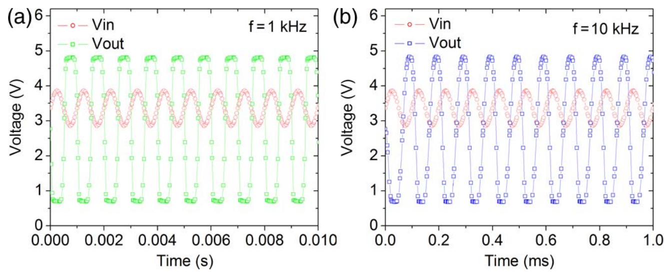

Fig. 14. Small-signal input and output waveforms of a common–source amplifier based on nc-Si TFTs when the input frequency is (a) 1 kHz and (b) 10 kHz.

formed by wire connecting nc-Si TFTs. The amplifier was tested with ac signals at different frequencies, and voltage gain $(v_{\rm out}/v_{\rm in})$ was calculated. The result is shown in Fig. 14. The output signal at low frequencies is essentially a sinusoid that is 180° out of phase with the input ac signal due to inversion. At higher frequencies, the phase difference changes owing to inverter lag.

The variation of the voltage gain with input frequency, as well as with inverter bias voltage, is shown in Fig. 15. The corresponding SPICE simulations were also performed and are included in the figures. In the first case, the input frequency was varied while fixing the supply voltage at 5 V. This resulted in the ac gain rising to a peak and then declining at higher frequencies. The maximum ac voltage gain of 10.2 resulted when the input ac signal frequency was 5 kHz. Simulations predict a similar trend with the gain showing a peak at 5 kHz. The reduction in gain at higher frequencies is probably due to the parasitic capacitances associated with wire connecting the circuit. The second case involved varying the supply voltage while the input frequency was fixed at 1 kHz. The ac gain monotonically increased with input frequency. Simulation results closely follow the measurements. These results are an improvement on amorphous-oxide-based amplifiers that use a larger supply voltage to realize a similar or lower ac gain [8].

VI. Conclusion

We have fabricated nc-Si TFTs with high hole and electron mobility values using low-temperature processing. Reducing

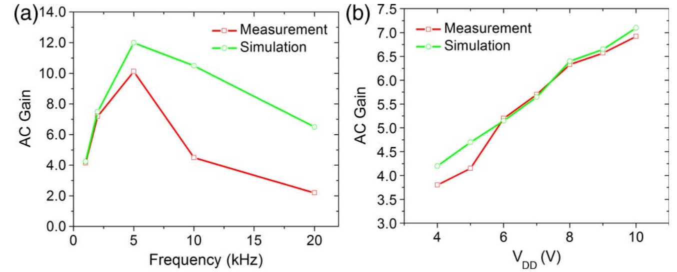

Fig. 15. Variation of voltage gain of the common–source amplifier with (a) input frequency (fixing the supply voltage at 5 V) and (b) supply voltage (input frequency fixed at 1 kHz). In both cases, measurements and SPICE simulation results are shown.

the oxygen impurity content in the channel resulted in ambipolar operation. Devices with nanoscale length and width were fabricated using two EBL steps and operated with no significant short-channel effects. The TFTs with Ti as the source/drain metal still exhibited ambipolar operation. This proves that the use of Cr is not essential, but rather, any metal with suitable work function can be employed. Increased threshold voltage and reduced mobility of the TFTs when operated with back-gate bias agree with the theory that most of conduction occurs at the bottom interface where silicon is mostly amorphous. The TFTs are very stable and exhibit low threshold voltage degradation. The submicron dimensions of the devices make them suitable for use in high-density architectures such as neuromorphic circuits.

A SPICE model was fit for the ambipolar nc-Si TFTs and was used to simulate an inverter circuit. These simulations closely matched the voltage transfer characteristics from a fabricated nc-Si TFT-based inverter. The ambipolar operation of the TFTs allowed a complementary inverter to be built using a single type of device. The voltage transfer characteristics of nc-Si inverters were discussed, and options to reduce the power dissipation were explored. The inverter's frequency response was measured by pulsing at different frequencies. The inverter was able to respond closely to the input until 2 MHz despite the associated large overlap capacitance values. The inverter was biased at turnover voltage and operated as an amplifier by applying a small ac signal in addition to the dc bias. The amplifier operated with no distortion over a wide range of frequency. AC gains up to 10 were measured by varying the frequency of operation.

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Anand Subramaniam (S'05) received the B.Tech. degree in electronics and communications from the National Institute of Technology, Calicut, India, in 2007. He is currently working toward the Ph.D. degree in electrical engineering at The University of Texas at Dallas, Richardson.

His current research interests include noncrystalline silicon transistors, neuromorphic circuits, spike-timing-based plasticity, and synaptic learning rules.

Kurtis D. Cantley (S'02–M'07) received the B.S.E.E. degree in 2005 from Washington State University, Pullman, and the M.S.E.E. degree in 2007 from Purdue University, West Lafayette, IN, where his research involved simulation of III–V materials in nanoscale transistors. He is currently working toward the Ph.D. degree in electrical engineering at The University of Texas at Dallas, Richardson, with funding from the National Defense Science and Engineering Graduate Fellowship.

While taking up the B.S.E.E. degree, he worked in the National Security Internship Program at Pacific Northwest National Laboratory. His research area is in nanoscale devices and materials for implementing artificial neural circuits.

Harvey J. Stiegler (S'70–M'80) received the B.S.E.E. degree from Texas Tech University, Lubbock, in 1973 and the M.S. and Ph.D. degrees from Rice University, Houston, TX, in 1985 and 1989, respectively.

After graduating from Texas Tech University, he served in the U.S. Air Force until 1979 and joined Texas Instruments (TI) Incorporated, Dallas, TX, in the same year. At TI, he was primarily involved in the development of nonvolatile memory products and dynamic RAMs, as well as analog and mixed signal products, as a Design Engineer and a Design Manager. He was elected TI Senior Member of the Technical Staff in 1993. In 2009, he joined The University of Texas at Dallas, Richardson, as a Research Scientist with the Department of Materials Science and Engineering.

Dr. Stiegler is a member of the American Physical Society and the American Association for the Advancement of Science.

Richard A. Chapman (M'78–SM'93–F'98) received the B.A., M.A., and Ph.D. degrees in physics from Rice University, Houston, TX, in 1954, 1955, and 1957, respectively.

After two years with General Electric Corporation, he joined Texas Instruments (TI) Incorporated, Dallas, TX, in 1959 and retired in 1998 as a TI Senior Fellow specializing in scaling of complementary metal–oxide–semiconductor transistors. From 1999 to 2007, he was a Consultant with TI. Since 2008, he has been a Research Scientist with The University of Texas at Dallas, Richardson.

Dr. Chapman is a Fellow of the American Physical Society. He was the General Chairman of the 1996 IEEE Symposium on Very Large Scale Integration Technology after having been a Program Chairman, a Secretary, and a Local Arrangements Chairman. In 1987, he was a corecipient of the IEEE Jack Morton Award for his 1978–1980 work on HgCdTe charge-transfer infrared sensor arrays.

Eric M. Vogel (M'93–SM'03) received the B.S. degree in electrical engineering from Pennsylvania State University, University Park, in 1994 and the Ph.D. degree in electrical engineering from North Carolina State University, Raleigh, in 1998.

He joined the National Institute of Standards and Technology, Gaithersburg, MD, and became the Leader of the CMOS and Novel Devices Group in 2001 and the Founding Director of the National Institute of Standards and Technology Nanofabrication Research Group in 2003. In August 2006, he joined The University of Texas at Dallas (UTD), Richardson, as an Associate Professor of materials science and engineering and electrical engineering. He was the Associate Director of the Texas Analog Center of Excellence and led UTD's portion of Southwest Academy for Nanoelectronics. He is currently a Professor with the School of Materials Science and Engineering, Georgia Institute of Technology, Atlanta. He has published more than 120 archival publications, written 4 book chapters, given more than 50 invited talks and tutorials, and has more than 80 contributed presentations. His research interests relate to devices and materials for future electronics, including advanced metal–oxide–semiconductor devices and materials and nanoelectronic devices.

Dr. Vogel is a member of the American Physical Society and Materials Research Society. He has been involved in several conferences, including the 2005 IEEE Semiconductor Interface Specialists Conference as the General Chair and the 2001 and 2008 IEEE International Reliability Physics Symposium as the High-k Program Chair.